Safety Summary

To ensure thorough understanding of all functions and to ensure efficient use of this instrument, please read the manual carefully before using. Note that Advantest bears absolutely no responsibility for the result of operations caused due to incorrect or inappropriate use of this instrument.

If the equipment is used in a manner not specified by Advantest, the protection provided by the equipment may be impaired.

- **Warning Labels**

  Warning labels are applied to Advantest products in locations where specific dangers exist. Pay careful attention to these labels during handling. Do not remove or tear these labels. If you have any questions regarding warning labels, please ask your nearest Advantest dealer. Our address and phone number are listed at the end of this manual.

  Symbols of those warning labels are shown below together with their meaning.

  DANGER: Indicates an imminently hazardous situation which will result in death or serious personal injury.

  WARNING: Indicates a potentially hazardous situation which will result in death or serious personal injury.

  CAUTION: Indicates a potentially hazardous situation which will result in personal injury or a damage to property including the product.

- **Basic Precautions**

  Please observe the following precautions to prevent fire, burn, electric shock, and personal injury.

  - Use a power cable rated for the voltage in question. Be sure however to use a power cable conforming to safety standards of your nation when using a product overseas.
  - When inserting the plug into the electrical outlet, first turn the power switch OFF and then insert the plug as far as it will go.
  - When removing the plug from the electrical outlet, first turn the power switch OFF and then pull it out by gripping the plug. Do not pull on the power cable itself. Make sure your hands are dry at this time.
  - Before turning on the power, be sure to check that the supply voltage matches the voltage requirements of the instrument.
  - Be sure to plug the power cable into an electrical outlet which has a safety ground terminal. Grounding will be defeated if you use an extension cord which does not include a safety ground terminal.
  - Be sure to use fuses rated for the voltage in question.
  - Do not use this instrument with the case open.

- Do not place objects on top of this product. Also, do not place flower pots or other containers containing liquid such as chemicals near this product.
- When the product has ventilation outlets, do not stick or drop metal or easily flammable objects into the ventilation outlets.
- When using the product on a cart, fix it with belts to avoid its drop.
- When connecting the product to peripheral equipment, turn the power off.

- **Caution Symbols Used Within this Manual**

Symbols indicating items requiring caution which are used in this manual are shown below together with their meaning.

DANGER: Indicates an item where there is a danger of serious personal injury (death or serious injury).

WARNING: Indicates an item relating to personal safety or health.

CAUTION: Indicates an item relating to possible damage to the product or instrument or relating to a restriction on operation.

- **Safety Marks on the Product**

The following safety marks can be found on Advantest products.

 : ATTENTION - Refer to manual.

 : Protective ground (earth) terminal.

 : DANGER - High voltage.

 : CAUTION - Risk of electric shock.

- **Replacing Parts with Limited Life**

The following parts used in the instrument are main parts with limited life.
Replace the parts listed below after their expected lifespan has expired.
Note that the estimated lifespan for the parts listed below may be shortened by factors such as the environment where the instrument is stored or used, and how often the instrument is used.

There is a possibility that each product uses different parts with limited life. For more information, refer to Chapter 1.

Main Parts with Limited Life

Part name	Life
Unit power supply	5 years
Fan motor	5 years
Electrolytic capacitor	5 years
LCD panel	6 years
LCD backlight	2.5 years
Floppy disk drive	5 years

- **Precautions when Disposing of this Instrument**

When disposing of harmful substances, be sure dispose of them properly with abiding by the state-provided law.

Harmful substances: (1) PCB (polycarbon biphenyl)
(2) Mercury
(3) Ni-Cd (nickel cadmium)
(4) Other
Items possessing cyan, organic phosphorous and hexadic chromium and items which may leak cadmium or arsenic (excluding lead in sol der).

Example: fluorescent tubes, batteries

Environmental Conditions

This instrument should be only be used in an area which satisfies the following conditions:

- An area free from corrosive gas
- An area away from direct sunlight
- A dust-free area
- An area free from vibrations

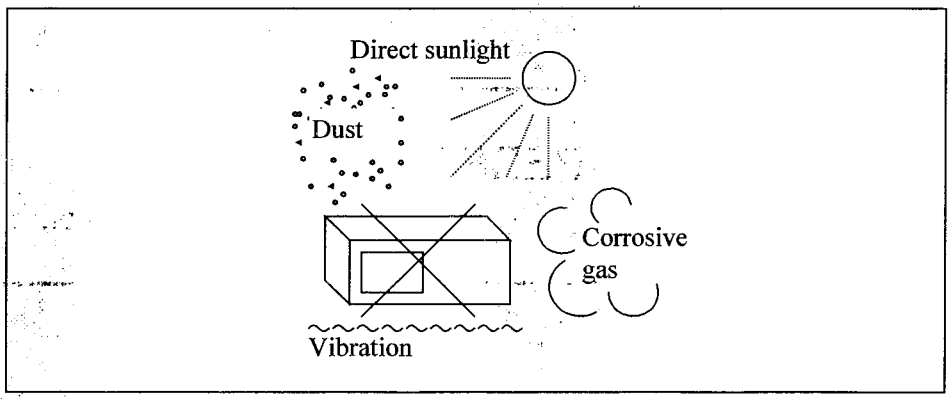


Figure-1 Environmental Conditions

- Instrument Placement

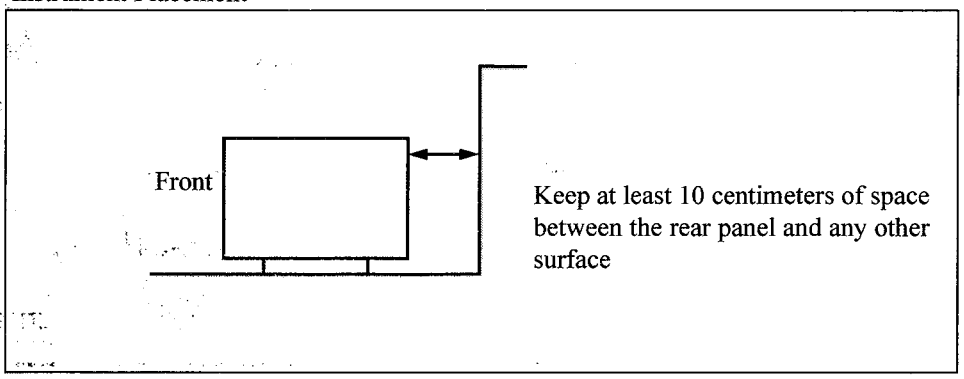


Figure-2 Instrument Placement

This instrument can be used safely under the following conditions:

- Altitude of up to 2000 m
- Installation Categories II
- Pollution Degree 2

R3265/3271 SPECTRUM ANALYZER MAINTENANCE MANUAL

TABLE OF CONTENTS

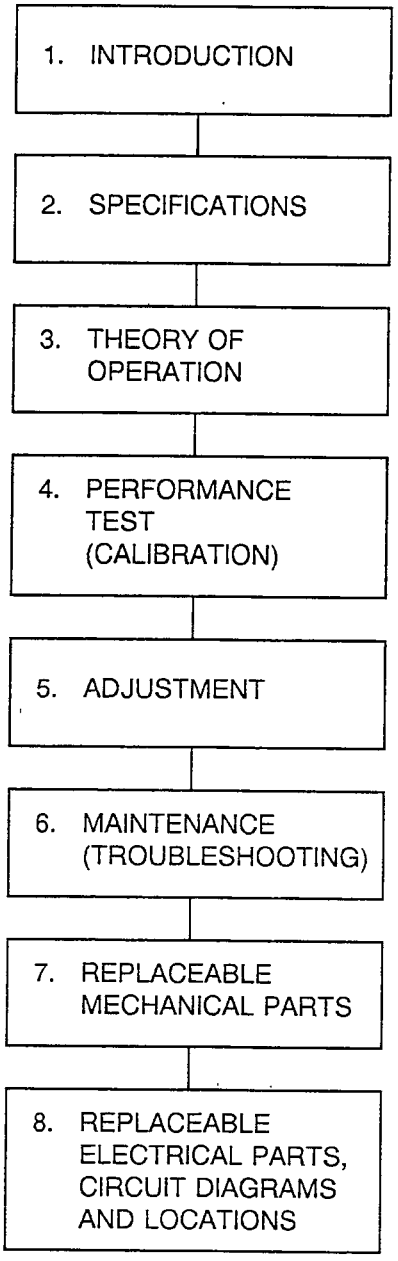
LIST OF ILLUSTRATIONS

LIST OF TABLES

1. INTRODUCTION

This chapter explains how to use this manual, and features of this spectrum analyzer.

1.1 How to Use This Manual



This chapter explains how to use this manual, and features of this spectrum analyzer.

This chapter lists the R3265/3271 specifications and accessories.

This chapter describes the operation of spectrum analyzer.

This chapter describes functions and cables necessary to the performance test for spectrum analyzer, and the method of performance test.

This chapter describes the method of adjusting the spectrum analyzer.

This chapter describes the method of troubleshooting the spectrum analyzer.

This chapter lists the mechanical part table of spectrum analyzer.

This chapter lists the parts list, circuit diagram, and layout drawing of specturm analyzer.

1.2 The R3265/3271 Spectrum Analyzer

The R3265/3271 series is a swept-turned spectrum analyzer with an analog-to-digital section for displaying and analyzing data. It operates in the following frequency, input, and display ranges:

Frequency range	:	100Hz to 8.0GHz (R3265) 100Hz to 26.5GHz (R3271)
Input range	:	-140dBm to +30dBm (R3265) -135dBm to +30dBm (R3271)
Display range	:	95dB

In these ranges, the analyzer features a maximum resolution of 10Hz, a residual FM (frequency modulation) of $3Hz_{p-p}$, and a noise sideband of -112dBc/Hz (at 10kHz from the carrier). The analyzer is equipped with GPIB remote control and a memory card fuction for saving and recalling waveform data and panel settings.

The anlayzer provides the following additional features:

- the ability to sweep over a wide frequency range: from 100Hz to 26.5GHz (for the R3271) or from 100Hz to 8GHz (for the R3265). The analyzer can also perform a log sweep over the range from 1kHz to 1GHz.
- high-frequency resolution of up to 10Hz, which permits analysis of adjacent signals and spurious signals at high frequencies.
- a precise measurement mode that uses the analyzer's built-in reference crystal to measure with 1Hz accuracy signals too weak to measure with a counter.
- a memory card that can store waveform and control settings.
- the ability to observe directly the electric field strength and the QP (quasi-peak) value.
- a digital memory CRT screen that displays signal traces without flickering. Digital memory also allows marker functions for accurate and easy reading of trace values.
- a zero span mode that allows the analyzer to be set to a sweep time of 50μs. This is useful for analyzing wave bursts and modulation.
- two independent channels of digital memory for simultaneous display of two traces.
- computer-controlled operation using a GPIB command set.

2. SPECIFICATIONS

This chapter describes the specifications and accessories for the R3265 and R3271.

2.1 R3265 Specifications

(1) Frequency Characteristics

● Frequency range	100Hz to 8GHz Frequency band — Higher harmonics degree 100Hz to 3.6GHz — 1 3.5GHz to 7.5GHz — 1 7.4GHz to 8GHz — 1
● Frequency read accuracy (Start, Stop, Center frequency, Marker frequency)	±(Frequency reading × Frequency reference accuracy + Span × Span accuracy +0.15× Resolution bandwidth + 10Hz) Span accuracy (Span > 2MHz) ±3% (Span ≤ 2MHz) ±5%
● Marker frequency counter Resolution Accuracy (S/N ≥25dB) Delta counter accuracy	 1Hz to 1kHz ±(Marker frequency × Frequency reference accuracy + 5Hz + 1LSD) ±(Δfrequency × Frequency reference accuracy + 10Hz + 2LSD)
● Frequency reference accuracy	±2 × 10^{-8} Cycles/Day ±1 × 10^{-7} Cycles/Year
● Frequency stability Residual FM (Zero span) Drift (After 1 hour warm-up)	 < $3Hz_{P-P}$ /0.1sec 50kHz < Span ≤ 2MHz, <2.5kHz × Sweep speed (min.) × N Span ≤ 50kHz, < 60Hz × Sweep speed (min.) × N
● Signal purity noise side band	

Offset	f ≤2.6GHz	f >2.6GHz
1kHz	< -100dBc/Hz	< -95dBc/Hz
10kHz	< -110dBc/Hz	< -108dBc/Hz
20kHz	< -110dBc/Hz	< -108dBc/Hz
100kHz	< -114dBc/Hz	< -110dBc/Hz

● Frequency span	
Linear span	
Range	200Hz to 8GHz, Zero span
Accuracy	±3% (Span > 2MHz), ±5% (Span≤2MHz)
Logarithmic span	
Range	1kHz to 1GHz (1, 2, or 3 decades can be selected)
Accuracy	±(10% + Stop frequency × 0.1%)
● Resolution bandwidth (-3dB)	
Range	10Hz to 3MHz, 1, 3, 10 sequence
Accuracy	±50% (Resolution bandwidth 10 to 100Hz, Digital IF) ±15% (Resolution bandwidth 100Hz to 1MHz) ±25% (Resolution bandwidth 3MHz, 30Hz) Note: 30Hz at 25°C ±10°C
Selectivity	< 15:1 (100Hz to 3MHz) < 20:1 (30Hz) 5:1 (10 to 100Hz, Digital IF) Nominal
Bandwidth (6dB)	200Hz, 9kHz, 120kHz (based on the CISPR specification)
● Video bandwidth	
Range	1Hz to 3MHz, 1, 3, 10 sequence

(2) Amplitude Range

● Measurement range	+30dBm to the average indicated noise level
● Maximum safe input	
Average continuous power (Input ATT≥10dB)	±30dBm (1W)
DC input	0 [V]
● Display range	10 × 10 div
Logarithmic	10, 5, 2, 1, 0.5, 0.2, 0.1 dB/div
Linear	(10% of the reference level)/div
QP logarithm	40dB (5dB/div)
● Reference level range	
Logarithmic	-140dBm to +60dBm (0.1dB increments)
Linear	2.2μV to 223V (approx. 1% step of the full scale)
● Input attenuator range	0 to 70dB (10dB step)

(3) Dynamic Range

● Maximum dynamic range	
1dB gain compression level	100MHz to 3.6GHz : 135dB - 1.55 × f(GHz)dB
Noise level	10MHz to 3.6GHz : 130dB - 1.55 × f(GHz)dB
Input frequency	
Distortion characteristics	
Higher harmonics	
100MHz to 3.6GHz	87dB
10MHz to 3.6GHz	82.5dB
> 3.5GHz	112dB
Tertiary intermodulation	
> 200MHz	93dB
> 10MHz	90dB
● Average display noise level (Resolution bandwidth 10Hz (Digital IF), Input attenuator 0dB, Average 20 times)	
Frequency range	
1kHz	-100dBm
10kHz	-110dBm
100kHz	-111dBm
1MHz to 3.6GHz	-{140 - 1.55 × f (GHz)}dBm
	-{145 - 1.55 × f (GHz)}dBm (Low noise mode)
3.5GHz to 8GHz	-135dBm
● 1dB gain compression	
> 200MHz	-5dBm (Mixer input level)
> 10MHz	-10dBm (Mixer input level)
● Spurious response	
Secondary higher harmonics distortion	
Frequency range	Mixer level
100MHz to 3.6GHz	-30dBm <-70dBc
10MHz to 3.6GHz	-30dBm <-60dBc
> 3.5GHz	-10dBm <-100dBc
Tertiary higher harmonics distortion	
Frequency range	Mixer level
200MHz to 3.6GHz	-30dBm <-70dBc
10MHz to 3.6GHz	-30dBm <-60dBc
> 3.5GHz	-30dBm <-75dBc
Image/Multiple/Band external response	
10MHz to 8GHz	< -70dBc

Residual response (No input signal, Input ATT 0dB, 50Ω terminate) 1MHz to 3.6GHz 300kHz to 8GHz	 < -100dBm < -90dBm

(4) Amplitude Accuracy

● Frequency response Flatness within the band (Input ATT 10dB) 100Hz to 3.6GHz 50MHz to 2.6GHz 3.5GHz to 7.5GHz 7.4GHz to 8GHz Additional error due to band switching Calibration signal as the reference (Input ATT 10dB)	 ±1.5dB ±1.0dB ±1.5dB ±1.5dB < +0.5dB ±3dB (100Hz to 8GHz)
● Calibration signal accuracy	-10dBm ±0.3dBm
● IF gain error (After self-calibration) 0dBm to -50dBm 0dBm to -80dBm ● Scale indication accuracy (After self calibration) Logarithmic Linear QP mode logarithmic	 ±0.3dB ±0.7dB ±0.2dB/1dB ±1dB/10dB ±1.5dB/90dB ±5% of reference level ±1.0dB/30dB, ±2dB/40dB ±1.0dB/40dB (25°C ±10°C)
● Error due to input attenuator switching (10dB as the reference; at 20 to 70 dB) Frequency range 0 to 8 GHz	 ±1.1dB/10dB step, Maximum 2.0dB
● Error due to resolution bandwidth switching (Resolution bandwidth: 300kHz, reference; after self-calibration)	 100Hz to 3MHz (analog IF) ±0.3dB 30Hz (analog IF) ±1dB 10Hz to 100Hz (digital IF) ±1.5dB

● Pulse quantization error (In pulse measurement mode, PRF > 700/Sweep time) Peak to peak	
Logarithmic	1.2dB (Resolution bandwidth ≤ 1MHz) 3dB (Resolution bandwidth = 3MHz)
Linear	4% of the reference level (Resolution bandwidth ≤ 1MHz) 12% of the reference level (Resolution bandwidth = 3MHz)

(5) Sweep

● Sweep time	
Zero span	50μs to 1000s, manual sweep
Span ≥ 200Hz	20ms to 1000s, manual sweep
Accuracy	±3%
● Trigger	Free run, Line, Single, Video, TV-H, TV-V, External

(6) Demodulation

● Spectrum demodulation	
Modulation type	AM, FM
Audio output	Internal speaker, earphone jack, sound volume adjustable
Demodulation duration	100ms to 1000s

(7) Input/Output

● RF input	
Connector	N-type female
Impedance	50Ω (nominal)
VSWR	
(Frequency setting input	< 1.5 : 1 (≤ 3.6GHz) (nominal)
ATT ≥ 10 dB)	< 2.0 : 1 (> 3.6GHz) (nominal)
LO radiation (average)	
Frequency setting (0 to 8GHz)	< −80dBm typical, input attenuation 10dB

<table>
<tr><td>● Calibration signal output
Connector
Frequency
Impedance
Amplitude</td><td>
BNC female, Front panel
25MHz × (1 ± Frequency reference accuracy)
50Ω (nominal)
−10dBm ± 0.3dB</td></tr>
<tr><td>● 10MHz frequency reference input/output
Connector
Impedance
Frequency range
Amplitude
Input range</td><td>
BNC female, Rear panel
50Ω (nominal)
10MHz × Frequency reference accuracy
0dBm ± 3dB
-5dBm to +5dBm</td></tr>
<tr><td>● 21.4MHz IF output
Connector
Impedance
Amplitude
3dB bandwidth</td><td>
BNC female, Rear panel
50Ω (nominal)
0dBm (Typ) in full scale
= Resolution bandwidth</td></tr>
<tr><td>● 421MHz IF output
Connector
Impedance
Gain, Noise factor, 3dB bandwidth
Frequency range
1MHz to 3.6GHz
3.5GHz to 8GHz</td><td>
BNC female, Rear panel
50Ω (nominal)
<table><tr><th>3dB bandwidth (nominal)</th><th>Noise factor (nominal)</th><th>Gain (nominal)</th></tr><tr><td>>15MHz
>30MHz</td><td>17dB
24dB</td><td>+6dB
-9dB</td></tr></table></td></tr>
<tr><td>● Video output
Connector
Impedance
(AC connection)
Amplitude (75Ω terminate)</td><td>
BNC female, Rear panel
75Ω (nominal)

Approx. $1V_{p-p}$ (Composite video signal)</td></tr>
<tr><td>● X axis, 2V/n GHz output
Connector
Impedance
X axis output
2V/n GHz</td><td>
BNC female, Rear panel
1kΩ (nominal), DC connection
approx. -5V to +5V
approx. 2V per 1GHz</td></tr>
<tr><td>● Y axis output
Connector
Impedance
Amplitude</td><td>
BNC female, Rear panel
220Ω (nominal)
approx. 2V in full scale</td></tr>
</table>

● Z axis output	
Connector	BNC female, Rear panel
Amplitude	TTL level
During sweep	High level
Retrace interval	Low level
● External trigger input	
Connector	BNC female, Rear panel
Impedance	10kΩ (nominal), DC connection
Trigger level	TTL level
● Gate input	
Connector	BNC female, Rear panel
Impedance	10 kΩ (nominal)
Sweep stop	During low mode at TTL level
Sweep	During high mode at TTL level
● Probe power	4-pin connector, Front panel
Voltage	+15V, -15V
Current	150mA each
● Voice output (Demodulation audio)	
Connector	Small-size monophonic jack, Front panel
Power output	Maximum 0.2W, 8Ω (nominal)
● GPIB	IEEE-488 bus connector
Plotters	R9833, HP7470A, HP7475A, HP7440A, HP7550A

(8) General Specifications

● Temperature and humidity	
During operation	0°C to 50°C
When stored	-20°C to 60°C
Relative Humidity	85% or below
● Power source	
During 100VAC operation	
Voltage	90V to 132V
Power consumption	400VA at maximum
Frequency	48Hz to 440Hz
During 220VAC operation	
Voltage	198V to 250V
Power consumption	400VA at maximum
Frequency	48Hz to 66Hz
● Weight	22kg (nominal) (Excluding optional blocks, front cover, and accessories)
● Dimensions	Approx. 177mm (Height) × 353mm (Width) × 450mm (Depth) (Excluding the handle, legs and front cover)

2.2 R3271 Specifications

(1) Frequency Characteristics

<table>
<tr><td>● Frequency range</td><td>100Hz to 26.5GHz
18GHz to 60GHz (Using an external mixer; Tuning available up to 325GHz)
Frequency band — Higher harmonics degree
100Hz to 3.6GHz — 1
3.5GHz to 7.5GHz — 1
7.4GHz to 15.4GHz — 2
15.2GHz to 23.3GHz — 3
23GHz to 26.5GHz — 4</td></tr>
<tr><td>● Frequency read accuracy
(Start, Stop, Center frequency, Marker frequency)</td><td>±(Frequency read x Frequency reference accuracy + Span × Span accuracy + 0.15 × Resolution bandwidth +10Hz)
Span accuracy (Span > 2MHz) ±3%
(Span ≤ 2MHz) ±5%</td></tr>
<tr><td>● Marker frequency counter
Resolution
Accuracy (S/N ≥ 25dB)

Delta counter accuracy</td><td>
1Hz to 1kHz
±(Marker frequency × Frequency reference accuracy + 5Hz × N + 1LSD)
±(Delta frequency × Frequency reference accuracy + 10Hz ×N +2LSD)</td></tr>
<tr><td>● Frequency reference accuracy</td><td>±2 × 10^{-8} /Day
±1 × 10^{-7} /Year</td></tr>
<tr><td>● Frequency stability
Residual FM (Zero span)
Drift
(After 1 hour warm-up)</td><td>
< 3Hz × N_{P-P} /0.1 sec
50kHz < Span ≤ 2MHz; < 2.5kHz × Sweep speed (min) × N
Span ≤ 50kHz; < 60Hz × Sweep speed (min) × N</td></tr>
<tr><td>● Signal purity noise side band</td><td>
<table>
<tr><th>Offset</th><th>f ≤ 2.6GHz</th><th>f > 2.6GHz</th></tr>
<tr><td>1kHz</td><td>< -100dBc/Hz</td><td>< (-95 + 20logN)dBc/Hz</td></tr>
<tr><td>10kHz</td><td>< -110dBc/Hz</td><td>< (-108 + 20logN)dBc/Hz</td></tr>
<tr><td>20kHz</td><td>< -110dBc/Hz</td><td>< (-108 + 20logN)dBc/Hz</td></tr>
<tr><td>100kHz</td><td>< -114dBc/Hz</td><td>< (-110 + 20logN)dBc/Hz</td></tr>
</table>
</td></tr>
</table>

● Frequency span Linear span Range Accuracy Logarithmic span Range Accuracy	 200Hz to 26.5GHz, Zero span ±3% (Span > 2MHz) ±5% (Span≤2MHz) 1kHz to 1GHz (1, 2, or 3 decades can be selected) ± (10% + Stop frequency × 0.1%)
● Resolution bandwidth (-3dB) Range Accuracy Selectivity Bandwidth (6dB)	 10Hz to 3MHz; 1, 3, 10 sequence ±50% (Resolution bandwidth 10 to 100Hz, Digital IF) ±15% (Resolution bandwidth 100Hz to 1MHz) ±25% (Resolution bandwidth 3MHz, 30Hz) Note: 30Hz at 25°C 10°C < 15:1 (100Hz to 3MHz) < 20:1 (30Hz) 5:1 (10 to 100Hz, Digital IF) Nominal 200Hz, 9kHz, 120kHz (based on the CISPR specification)
● Video bandwidth Range	 1Hz to 3MHz; 1, 3, 10 sequence

(2) Amplitude Bandwidth

● Measurement range	+30dBm to Average indication noise level
● Maximum safe input Average continuous power (Input ATT≥10dB) DC input	 +30dBm (1W) 0 [V]
● Display range Logarithmic Linear QP logarithmic	10 × 10 div 10, 5, 2, 1, 0.5, 0.2, 0.1 dB/div (10% of the reference level) /division 40dB (5dB/div)
● Reference level range Logarithmic Linear	 -140dBm to +60dBm (0.1dB step) 2.2μV to 223V (approx. 1% step of the full scale)
● Input attenuator range	0 to 70 dB (10dB step)

(3) Dynamic Range

● Maximum dynamic range 1dB gain compression level noise level Input frequency Distortion characteristics Higher harmonics 10MHz to 3.6GHz 10MHz> 3.5GHz Tertiary intermodulation > 10MHz	 10MHz to 3.6GHz: 130dB − 1.55 × f(GHz) dB 85dB 110dB 90dB
● Average indication noise level (Resolution bandwidth 10Hz (Digital IF), Input attenuator 0dB, Average 20 times) Frequency range 1kHz 10kHz 100kHz 1MHz to 3.6GHz 3.5GHz to 7.5GHz 7.5GHz to 15.4GHz 15.2GHz to 23.3GHz 23GHz to 26.5GHz	 -100dBm -110dBm -111dBm -{135 - 1.55 × f (GHz)}dBm -130dBm -123dBm -116dBm -110dBm
● 1dB gain compression > 10MHz	 -5dBm (Mixer input level)
● Spurious response Secondary higher harmonics distortion Frequency range 10MHz to 3.6GHz 10MHz> 3.5GHz Tertiary higher harmonics distortion Frequency range 10MHz to 3.6GHz 10MHz> 3.5GHz Image/Multiple/Band external response 10MHz to 18GHz 10MHz to 23GHz 10MHz to 26.5Hz	 Mixer level -30dBm < -70dBc -10dBm < -100dBc Mixer level -30dBm < -70dBc -30dBm < -75dBc < -70dBc < -60dBc < -50dBc

Residual response (No input signal, Input ATT 0dB, 50Ωterminate) 1MHz to 3.6GHz 300kHz to 26.5GHz	 < -100dBm < - 90dBm

(4) Amplitude Accuracy

● Frequency response Flatness within the band (Input ATT 10dB) 100Hz to 3.6GHz 50MHz to 2.6GHz 3.5GHz to 7.5GHz 7.4GHz to 15.4GHz 15.4GHz to 23.3GHz 23GHz to 26.5GHz Additional error due to band switching When the calibration signal is used as the reference (Input ATT 10dB)	 ±1.5dB ±1.0dB ±1.5dB ±3.5dB ±4.0dB ±4.0dB ±0.5dB ±5dB (100Hz to 26.5GHz)
● Calibration signal accuracy	-10dB ±0.3dBm
● IF gain error (After self-calibration) 0dBm to -50dBm 0dBm to -80dBm ● Scale indication accuracy (after self-calibration) Logarithmic Linear QP mode logarithmic	 ±0.3dB ±0.7dB ±0.2dB/1dB ±1dB/10dB ±1.5dB/90dB ±5% of the reference level ±1.0dB/30dB ±2dB/40dB ±1.0dB/40dB (25°C ±10°C)
● Input attenuator Switching error (Based on 10dB; in the range of 20 to 70 dB) Frequency range 0 to 12.4 GHz 12.4 to 18 GHz 18 to 26.5 GHz	 ±1.1dB/10dB step; Maximum 2.0dB ±1.3dB/10dB step; Maximum 2.5dB ±1.8dB/10dB step; Maximum 3.5dB
● Resolution bandwidth switching error (Resolution bandwidth: 300kHz; After self calibration)	 100Hz to 3MHz: ±0.3dB 30Hz : ±1dB 10 to 100 Hz (Digital IF) ±1.5dB

● Pulse quantization error (In pulse measurement mode: PRF > 700/Sweep time) Peak to peak Logarithmic Linear	 1.2dB (Resolution bandwidth ≤ 1MHz) 3dB (Resolution bandwidth = 3MHz) 4% of the reference level (Resolution bandwidth ≤ 1MHz) 12% of the reference level (Resolution bandwidth = 3MHz)

(5) Sweep

● Sweep time Zero span Span ≥ 200Hz Accuracy	 50μs to 1000s, Manual sweep 20ms to 1000s, Manual sweep ±3%
● Trigger	Free run, Line, Single, Video, TV-H, TV-V, External

(6) Demodulation

● Spectrum demodulation Modulation type Audio output Demodulation duration	 AM, FM Internal speaker, earphone jack, sound volume adjustable 100ms to 1000s

(7) Input/Output

● RF input Connector Impedance VSWR (Input ATT ≥ 10dB, frequency setting) LO radiation (average) Frequency setting 0 to 26.5GHz	 N-type, female (can be converted into SMA type) 50Ω (nominal) < 1.5:1 (≤ 3.6GHz) (nominal) < 2.5:1 (> 3.6GHz) (nominal) < -80dBm Typ, Input ATT 10dB
● First LO output Connector Impedance Frequency range Amplitude	 SMA, female, Front panel 50Ω (nominal) 3.921 to 7.921 GHz ±5dB or above

<table>
<tr><td>● Calibration signal output
Connector
Frequency
Impedance
Amplitude</td><td>
BNC female, Front panel
25MHz × (1 ± Frequency reference accuracy)
50Ω (nominal)
−10dBm ± 0.3dB</td></tr>
<tr><td>● 10MHz frequency reference input/output
Connector
Impedance
Frequency range
Amplitude
Input range</td><td>

BNC female, Rear panel
50Ω (nominal)
10MHz × Frequency reference accuracy
0dBm ± 3dB
-5dBm to +5dBm</td></tr>
<tr><td>● 21.4MHz IF output
Connector
Impedance
Amplitude
3dB bandwidth</td><td>
BNC female, Rear panel
50Ω (nominal)
0dBm (Typ) in full scale
= Resolution bandwidth</td></tr>
<tr><td>● 421MHz IF output
Connector
Impedance
Gain, Noise factor, 3dB bandwidth
Frequency range
1MHz to 3.6GHz
3.5GHz to 8GHz
7.4GHz to 15.4GHz
15.2GHz to 23.3GHz
23GHz to 26.5GHz</td><td>
BNC female, Rear panel
50Ω (nominal)<table><tr><th>3dB bandwidth (nominal)</th><th>Noise factor (nominal)</th><th>Gain (nominal)</th></tr><tr><td>>15MHz</td><td>24dB</td><td>-5dB</td></tr><tr><td>>30MHz</td><td>24dB</td><td>-4dB</td></tr><tr><td>>35MHz</td><td>30dB</td><td>-10dB</td></tr><tr><td>>40MHz</td><td>38dB</td><td>-18dB</td></tr><tr><td>>50MHz</td><td>44dB</td><td>-24dB</td></tr></table></td></tr>
<tr><td>● Video output
Connector
Impedance
(AC connection)
Amplitude (75Ω terminate)</td><td>
BNC female, Rear panel
75Ω (nominal)

Approx. 1V_{P-P} (Composite video signal)</td></tr>
<tr><td>● X axis, 2V/n GHz output
Connector
Impedance
X axis output
2V/n GHz</td><td>
BNC female, Rear panel
1kΩ (nominal), DC connection
approx. -5V to +5V
approx. 2V per 1GHz</td></tr>
<tr><td>● Y axis output
Connector
Impedance
Amplitude</td><td>
BNC female, Rear panel
220Ω (nominal)
approx. 2V in full scale</td></tr>
</table>

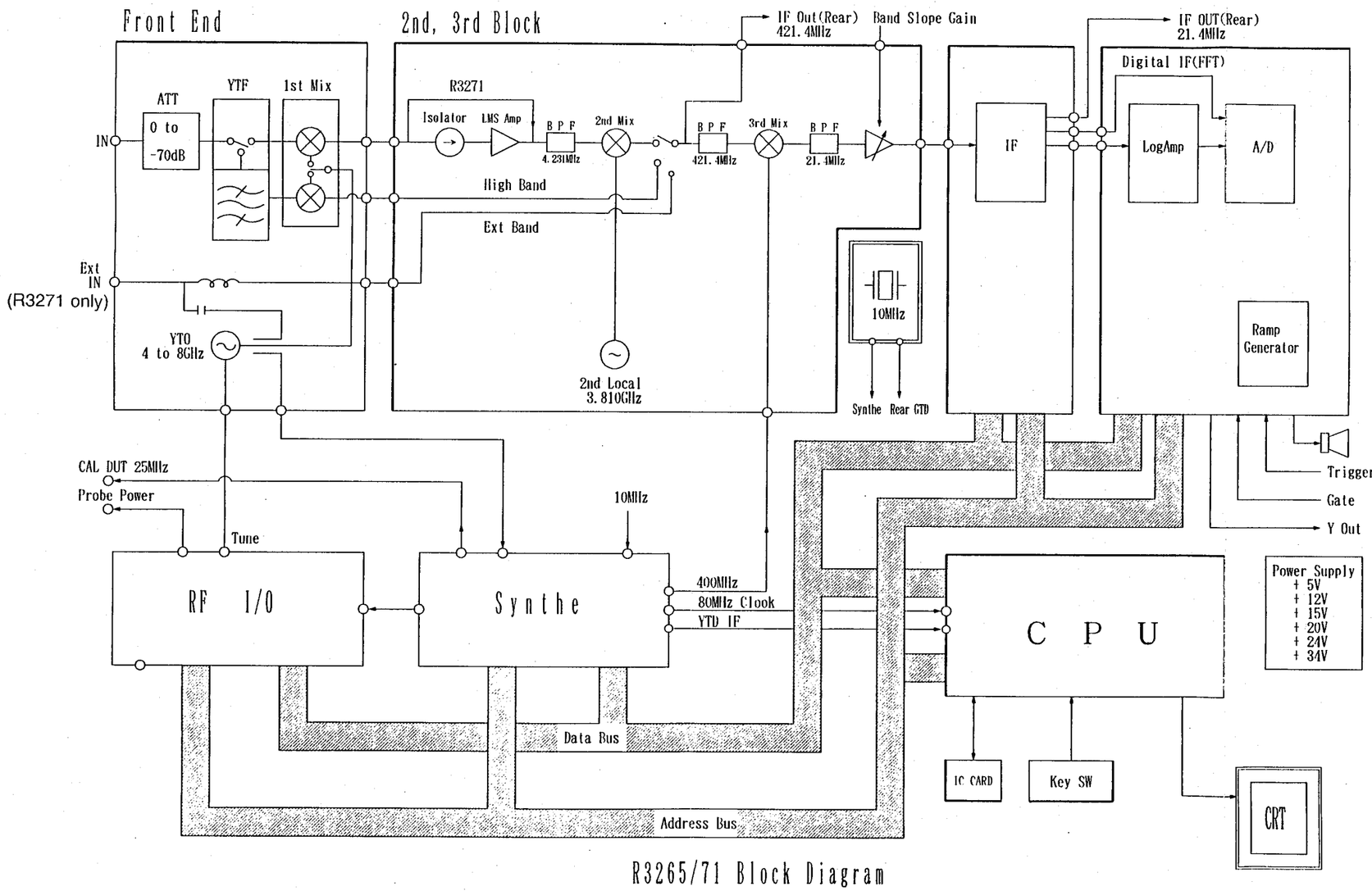
● Z axis output	
Connector	BNC female, Rear panel
Amplitude	TTL level
During sweep	High level
Retrace interval	Low level
● External trigger input	
Connector	BNC female, Rear panel
Impedance	10kΩ (nominal), DC connection
Trigger level	Trigger at the TTL level raise
● Gate input	
Connector	BNC female, Rear panel
Impedance	10kΩ (nominal)
Sweep stop	During low mode at TTL level
Sweep	During high mode at TTL level
● Probe power	4-pin connector, Front panel
Voltage	+15V, -15V
Current	Max. 150mA each
● Voice output (Demodulation audio)	
Connector	Small-size monophonic jack, Front panel
Power output	Maximum 0.2W, 8Ω (nominal)
● GPIB	IEEE-488, Bus connector
Plotters	R9833, HP7470A, HP7475A, HP7440A, HP7550A

(8) General Specifications

● Temperature and Humidity	
During operation	0°C to 50°C
When stored	-20°C to 60°C
Relative Humidity	85% or below
● Power source	
During 100VAC operation	
Voltage	90V to 132V
Power consumption	400VA at maximum
Frequency	48Hz to 440Hz
During 220VAC operation	
Voltage	198V to 250V
Power consumption	400VA at maximum
Frequency	48Hz to 66Hz
● Weight	22kg (nominal) (excluding optional blocks, front cover, and accessories)
● Dimensions	Approx. 177mm (height) × 353mm (width) × 450mm (depth) (excluding the handle, legs, and front cover)

3. THEORY OF OPERATION

3.1 GENERAL BLOCK DIAGRAMS



R3265/71 Block Diagram

Figure 3.1-1 R3265/3271 Block Diagram

3.2 Front END BLOCK

3.2.1 Block Diagram

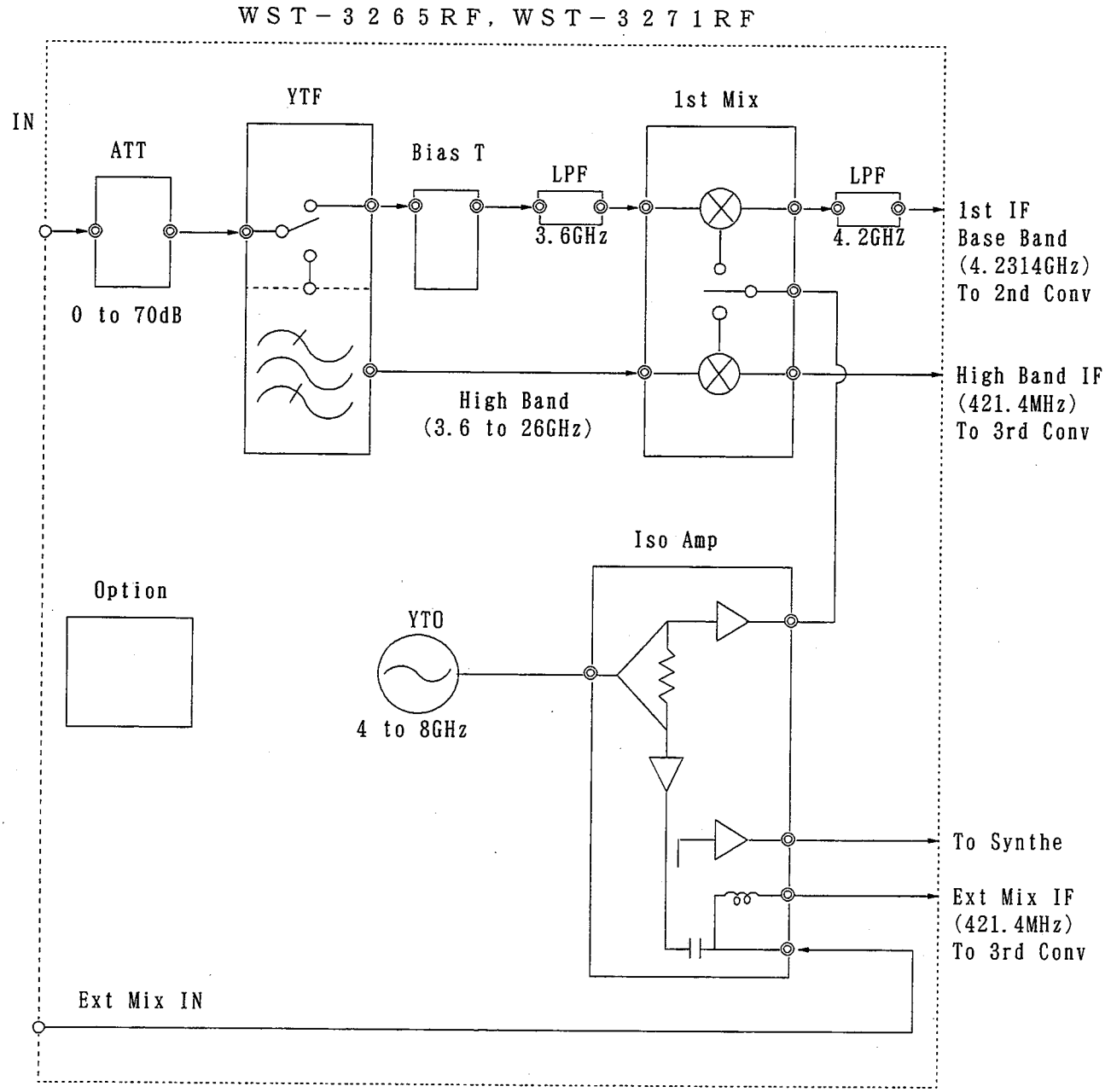


Figure 3.2-1 Front End Block Diagram

3.2.2 INPUT ATTENUATOR

(1) R3271 (DAT-001882-1)

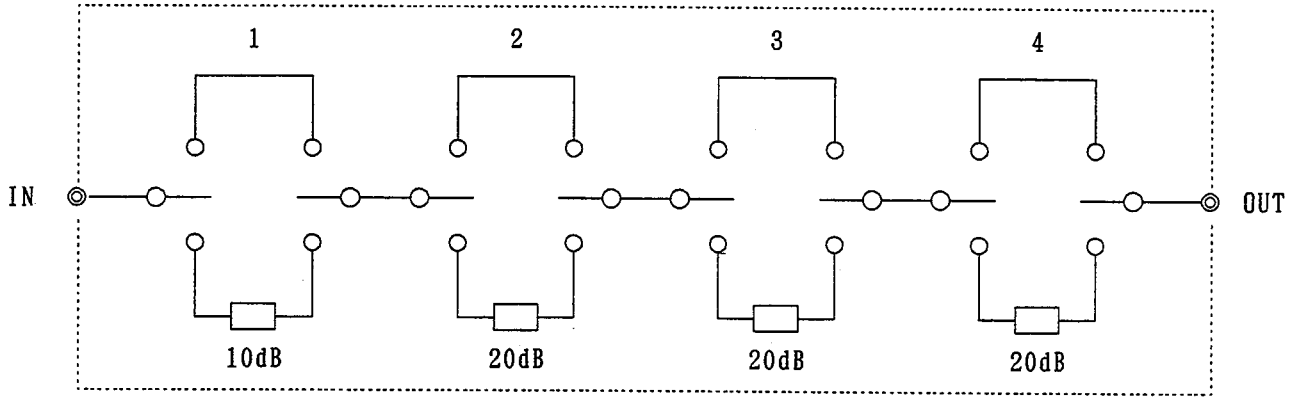


Figure 3.2-2 R3271 Input Attenuator

	1	2	3	4
0dB				
10dB	ON			
20dB				ON
30dB	ON			
40dB		ON		ON
50dB	ON	ON		ON
60dB		ON	ON	ON
70dB	ON	ON	ON	ON

(2) R3265 (DAT-001936-1)

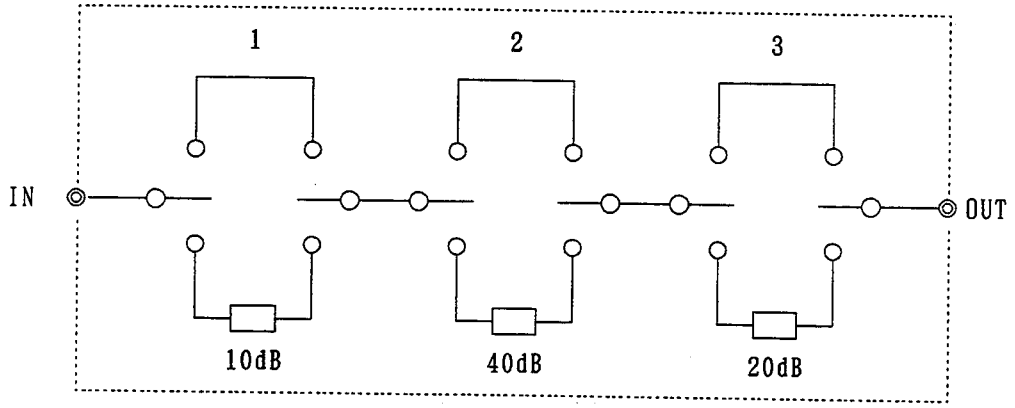


Figure 3.2-3 R3265 Input Attenuator

	1	2	3
0dB			
10dB	ON		
20dB			ON
30dB	ON		
40dB		ON	
50dB	ON	ON	
60dB		ON	ON
70dB	ON	ON	ON

3.2.3 YTF (YIG Tuned Filter)

YTF(YIG Tuned Filter) TOP2201(R3271), TOP2202(R3265)

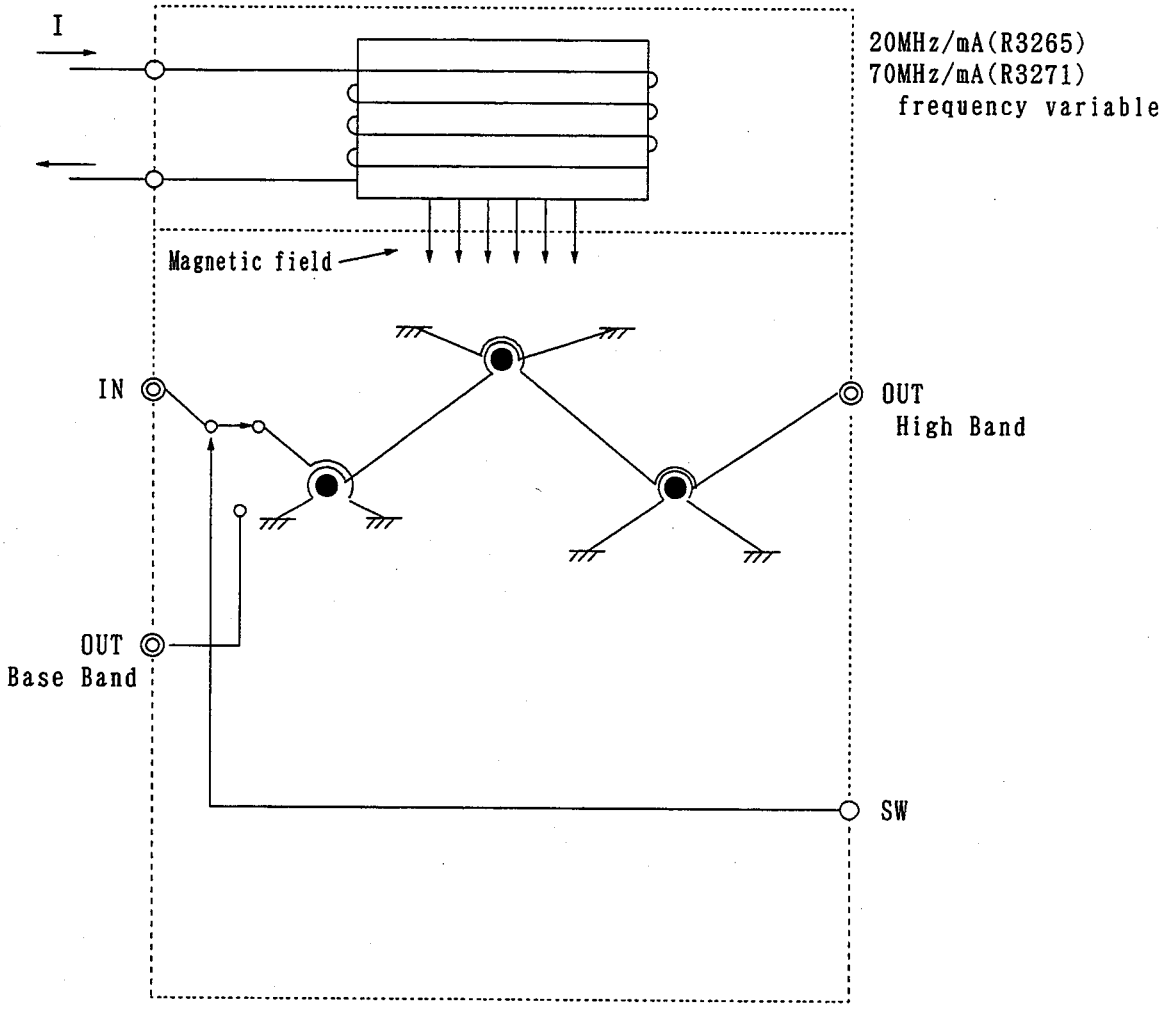


Figure 3.2-4 YIG Tuned Filter

The YTF consists of YIG couplings shifted by 90° as shown above. Introducing a current through the tuning terminal generates a magnetic field.

While the YIG varies its resonance frequency in proportion to the intensity of this magnetic field, the YTF makes a variable-frequency bandpass filter by controlling the intensity of the magnetic field (current).

A built-in switch selects the input signal source between the base band and the high band.

3.2.4 Bias-Tee

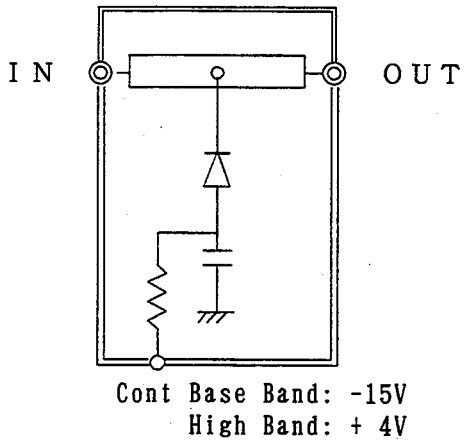


Figure 3.2-5 Bias-Tee

In the high band operation, the bias-tee circuit is used to prevent signals (particularly, 421.4MHz) form leaking to the base band.

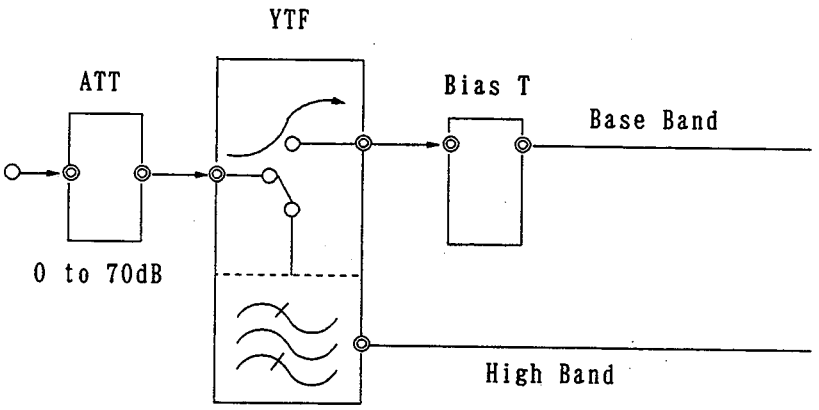


Figure 3.2-6 YTF Band Selector Switch

3.2.5 First Mixer

1st Mix THD293(R3271), THD294(R3265)

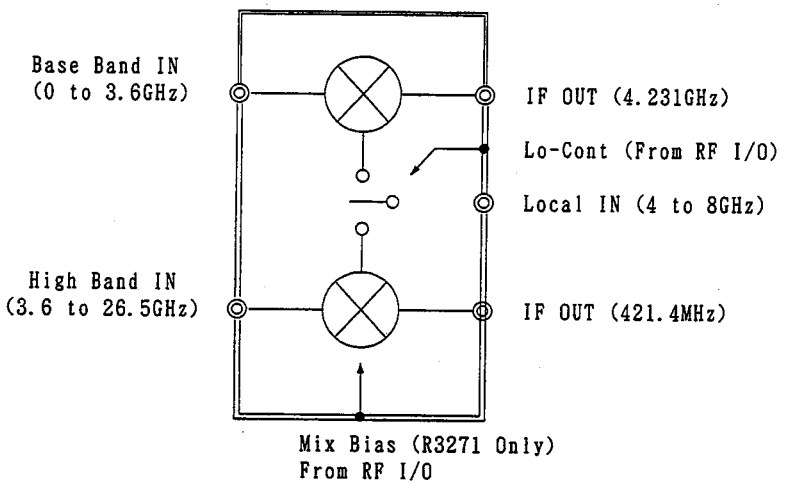


Figure 3.2-7 1st Mixer

A base-band and a high-band mixer are enclosed in a single casing. Local signals from the YTO are switched to either the base or high band by a LO-CONT signal from an internal switch.

The mixing bias for the high band setting is selectable using the number of degrees of the local signal. It is not necessary for R3265 to use the mixing bias for the base-band mixer.

LO-CONT base band : −2.8V
high band : +1.8V

3.2.6 Isolation Amplifier

Isolation amplifier (THD290, common to both R3265 and R3271)

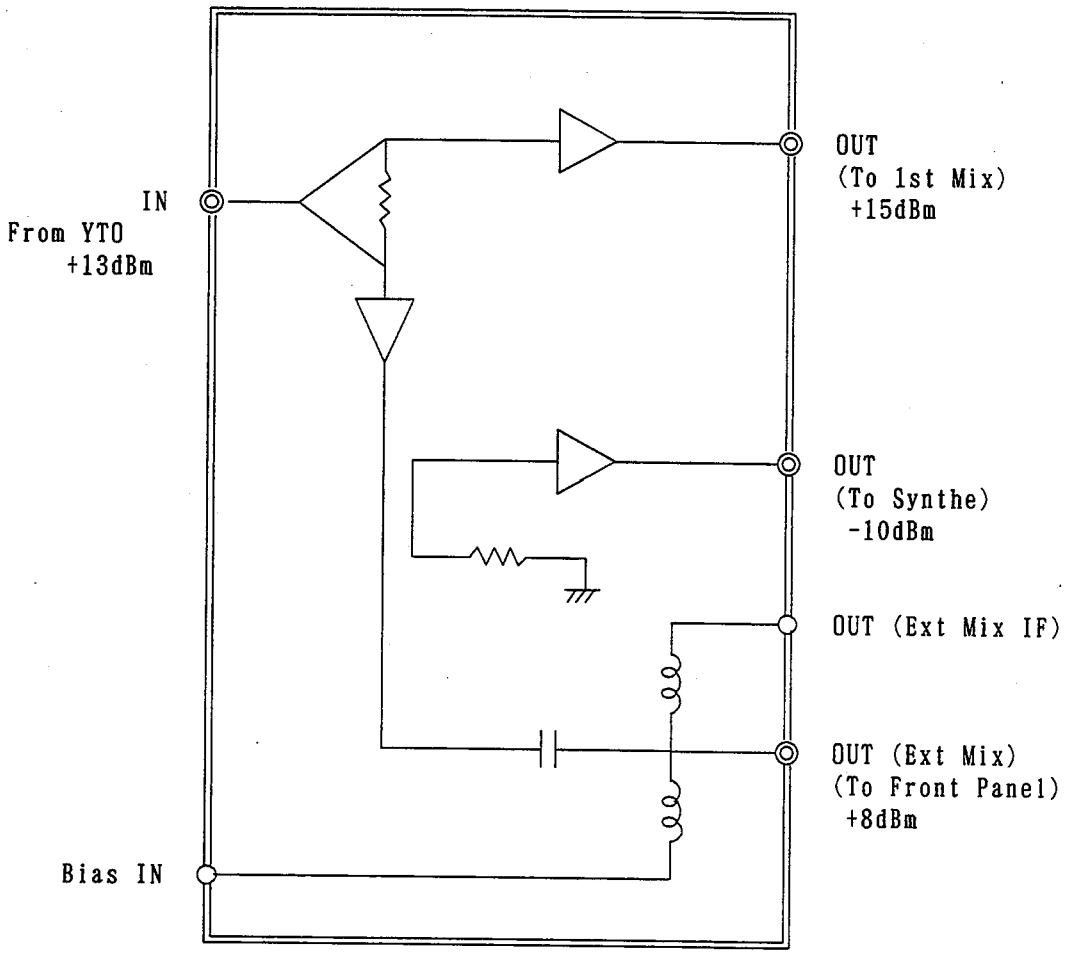


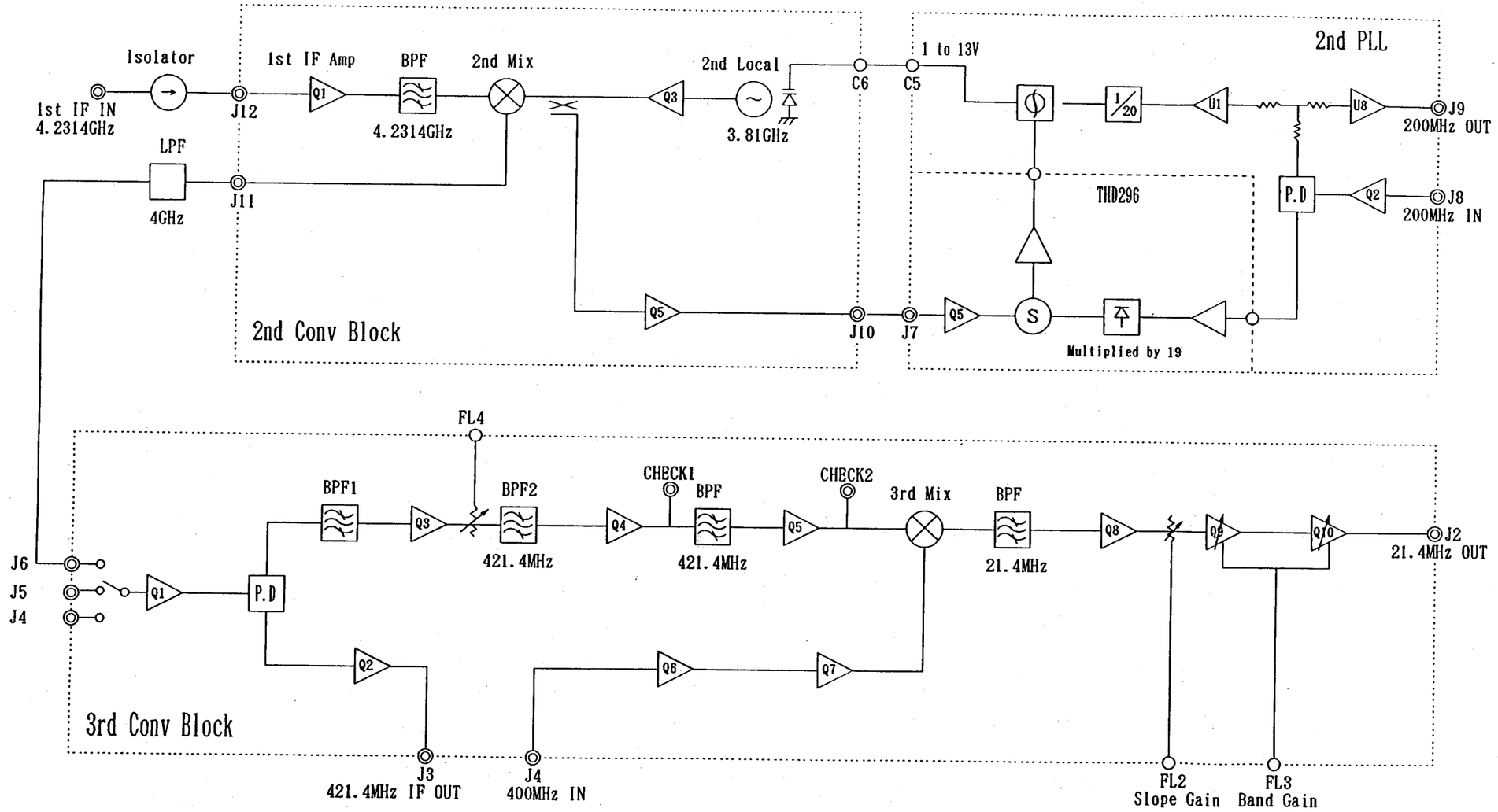
Figure 3.2-8 Isolation Amplifier

The isolation amplifier distributes the signal from the YTO (4-8GHz) to the first mixer, external mixer, and synthesizers at appropriate levels.

It also maintains an isolation between the individual ports to suppress unwanted responses. The External mixer output holds a bias circut and a isolation circut separated with local and IF.

3.3 SECOND AND THIRD CONVERTER BLOCKS

3.3.1 Block Diagram



J6: Base Band
J5: High Band
J4: Ext Band

P.D.: Power Divider

Isolator, 1st IF Amp: R3265 Only

Figure 3.3-1 2nd, 3rd Conv Block

3.3.2 Second Converter Operation Description

(1) Second converter block

The base-band IF signal (4.2314GHz) from the first mixer are routed differently between the R3265 and the R3271.

R3265 : The signal passes through the isolator and the first IF amplifier.

R3271 : The signal does not pass through the first IF amplifier.

The IF signal input from the J12 connector passes through a bandpass filter (using a dielectric resonator) before it enters the second mixer.

In the second fixer, the input IF signal is mixed with a second local signal (3.810GHz) to produce a second IF signal (421.4MHz), which is then output from the J11 connector.

Why the isolator and the first IF amplifier are used

In the R3265, a first IF amplifier (ultra-low noise amplifier: gain +15dB, N/F 1dB) is inserted in the first stage of the second converter block to achieve −145dB sensitivity.

(2) Second local oscillator (3.810GHz)

The second local oscillator is a PLL operating on a 200MHz reference signal.

In operation, the 200MHz reference signal from the synthesizer block is input to the second PLL, where it is distributed to the sampler and the phase detector.

On entering the sampler, the 200MHz signal is multiplied by 19 by SRD to produce a 3.800GHz signal.

In the sampler, the 3.800GHz signal is combined with the second local signal (3.810GHz) input from the J7 connector to produce a sampler IF signal (10MHz) for input to the phase detector in the second PLL.

On entering the second PLL, the 200MHz signal is divided by 20 to 10MHz, which is subsequently compared with the sampler IF signal by the phase detector.

The resultant control voltage signal (from +1V to +13V) is applied to the tuning varactor in the second local oscillator to lock it at 3.810GHz.

3.3.3 Third Converter Operation Description

(1) Input selector

The three possible sources of the input IF signal (421.4MHz) of the third converter are the base band, high band, and external mixer. A built-in pin diode switch electrically selects these sources from among the J4, J5, and J6 connectors.

(2) Third mixer

The input IF signal (421.4MHz) passes through an amplifier (Q1) before it is distributed to the third mixer and the rear panel IF OUT connector (J3).

The IF signal led to the third mixer is sent through a BPF1, a BPF2, and an amplifier to the third mixer.

In the third mixer, the input signal is mixed with the third local signal (400MHz) input from the J1 connector to produce a third IF signal (21.4MHz).

(3) Gain control amplifier

The third IF signal (21.4MHz) passes through a BPF and an amplifier, then through a slope gain amplifier and a band gain amplifier before it is output to the IF block through the J2 connector.

Slope gain amplifier

Corrects the system's frequency characteristics. The correction values are stored in EEPROM.

Band gain amplifier

Corrects Conversion losses of the each band in the first mixer. The correction values are stored in EEPROM.

3.3.3 Third Converter Operation Description

(1) Input selector

The three possible sources of the input IF signal (421.4MHz) of the third converter are the base band, high band, and external mixer. A built-in pin diode switch electrically selects these sources from among the J4, J5, and J6 connectors.

(2) Third mixer

The input IF signal (421.4MHz) passes through an amplifier (Q1) before it is distributed to the third mixer and the rear panel IF OUT connector (J3).

The IF signal led to the third mixer is sent through a BPF1, a BPF2, and an amplifier to the third mixer.

In the third mixer, the input signal is mixed with the third local signal (400MHz) input from the J1 connector to produce a third IF signal (21.4MHz).

(3) Gain control amplifier

The third IF signal (21.4MHz) passes through a BPF and an amplifier, then through a slope gain amplifier and a band gain amplifier before it is output to the IF block through the J2 connector.

Slope gain amplifier

Corrects the system's frequency characteristics. The correction values are stored in EEPROM.

Band gain amplifier

Corrects Conversion losses of the each band in the first mixer. The correction values are stored in EEPROM.

3.4 IF BLOCK

3.4.1 Block Diagram

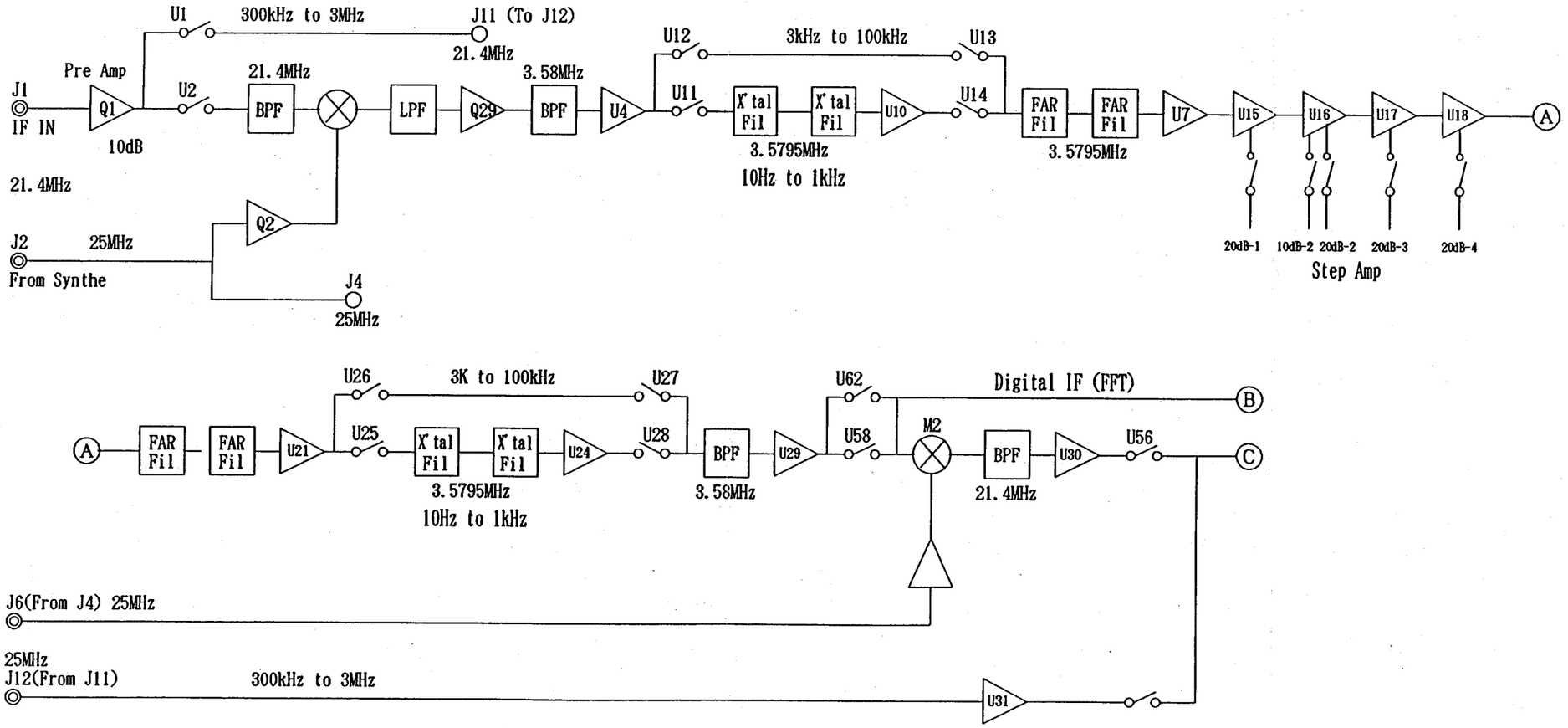


Figure 3.4-1 IF Block (1)

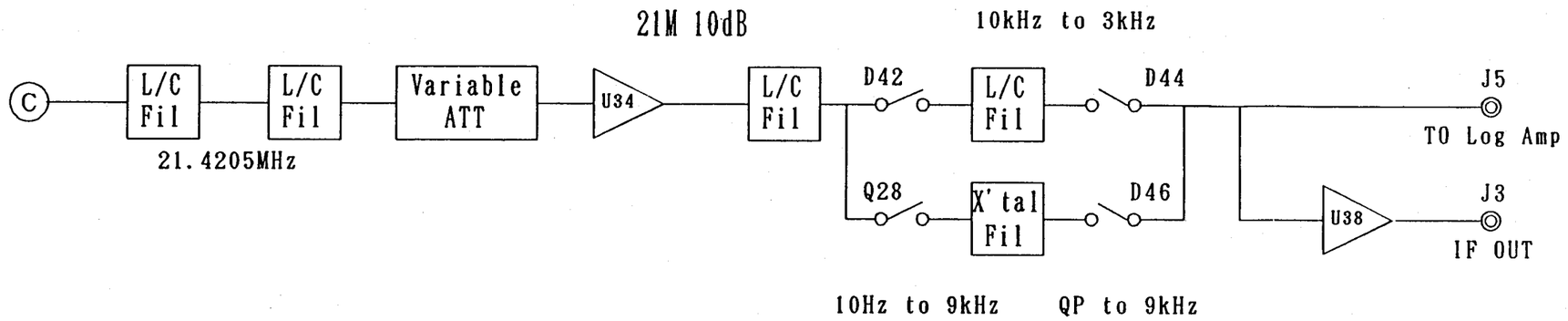


Figure 3.4-2 IF Block (2)

3.4.2 IF Filter Operation Description

Basic Arrangement

① RBW (Resolution Bandwidth)

10Hz to 3MHz (1 to 3 steps). Setting of RBWs of 300kHz to 3MHz (3dB) and 1MHz (6dB) is accomplished by the use of DAC (U45), U44, and U46.

With RBW settings of 300kHz to 3MHz, the input IF signal does not pass through the step amplifier circuit. Changing reference levels are lifted by the use of U34 (21MHz 10dB) and the log amplifier.

Setting of RBWs of 10Hz to 100kHz (3dB), and 200Hz, 9kHz, and 120kHz (6dB) is accomplished by the use of latch IC (U39) and U40 to U43.

In digital IF operation, the three RBW settings of 10Hz, 30Hz, and 100Hz are converted to 900Hz at the final and the same way as the RBW setting of 300Hz in the IF Filter.

DAC (U63), working like a variable attenuator, is set the same way as U54 (see the step amplifier description below).

② AR (Acoustic Resonant) Filter

The FAR filter is a resonance filter made of a lithium tantalate material. In the R3265/71 the AR filter covers RBW settings of 3kHz to 100kHz.

③ Step Amplifier

The step amplifier consists of 10dB (1), 20dB (4), 21MHz 10dB (1), and a variable attenuator (1). These amplification levels are selectable with the input attenuator and the reference level setting. The variable attenuator is automatically set by DAC (U54) according to the input attenuator, reference level, and calibration data.

Table 2 gives the relationship between the reference level and the step amplifier.

④ Preamplifier

The preamplifier is installed to improve the IF noise figure. When the Low Noise Mode option available from the spectrum analyzer menu is turned ON, the 10dB preamplifier (Q1) is set ON by latch IC (U39) and U3.

This function is available only with the R3265.

3.4.3 RBW Step

Table 3.4-1 RBW Step Table

		U39 Pin No														
Filter	RBW	3	64	61	60	56	55	54	4	62	59	6	7	8	11	9
L/C	3MHz											○	○	○		
	1MHz											○	○	○		
	300kHz											○	○	○		
FAR	100kHz												○	○		
	30kHz	○											○	○		
	10kHz		○										○	○		
	3kHz			○									○	○	○	
X'tal	1kHz			○											○	
	300Hz			○	○										○	
	100Hz			○		○									○	
	30Hz			○			○								○	
	10Hz			○				○							○	
QP (EMC)	1MHz											○	○	○		
	120kHz								○				○	○		
	9kHz									○			○	○	○	
	200Hz			○							○				○	
Digital IF				○	○											○

Note : In the table above, columns marked by a circle indicate the state of a U39 pin being at 0V; blank columns indicate the state of a U39 pin being at +5V.

- 6Pin : 0V U1, 55 (ON) U2, 56 (OFF)
- 7Pin : 0V U12, 13 (ON) U11, 14 (OFF)
- 8Pin : 0V U26, 27 (ON) U25, 28 (OFF)
- 11Pin : 0V Q28, D46(ON) D42, 44 (OFF)
- 9Pin : 0V U62 (ON) U58 (OFF)

3.4.4 Relationship between the Reference Level and Step Amplifier

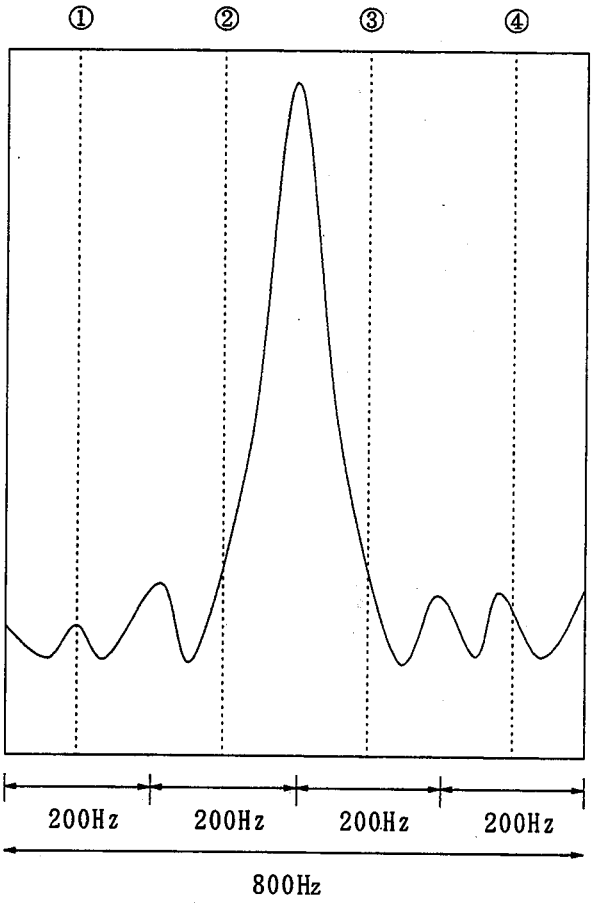
Table 3.4-2 Relationship between the REF LEVEL and Steep AMP

Low Noise	RBW	REF LEVEL	10dB PreAmp	10dB −2	20dB −1	20dB −2	20dB −3	20dB −4	21M 10dB
OFF	10Hz	0dBm							
		−10		○					
		−20			○				
		−30		○	○				
	100kHz	−40			○	○			
		−50		○	○		○		
	120kHz	−60			○	○	○		
	9kHz	−70		○	○		○	○	
	200Hz	−80 to		○	○		○	○	○
	300kHz								
		0dBm							
	3MHz								○
	(3dB)	−10 to							
	1MHz								
	(6dB)								
ON	10Hz	−10	○						
		−20	○	○					
		−30	○		○				
		−40	○	○	○				
	100kHz	−50	○		○	○			
		−60	○	○	○		○		
	120kHz	−70	○		○	○	○		
	9kHz	−80	○	○	○		○	○	
	200Hz	−90 to	○	○	○		○	○	○
	300kHz								
		0dBm	○						
	3MHz								
	(3dB)	−20 to	○						○
	1MHz								
	(6dB)								

Note : In the table above, columns marked by a circle indicate that the step amplifier is ON when the input attenuator setting is 10dB; blank columns indicate that it is OFF.

3.4.5 Digital IF Description

Example : 800Hz span



The digital IF (FFT) mode setting places the spectrum analyzer into the zero span state. In this state, the analyzer converts timebase data from analog to digital while moving the center frequency by 200Hz at a time as shown above, with the resultant digital data being subjected to FFT (with a Gaussian window function) for subsequent synthesized display.

3.5 LOG AMPLIFIER BLOCK

3.5.1 Block Diagram

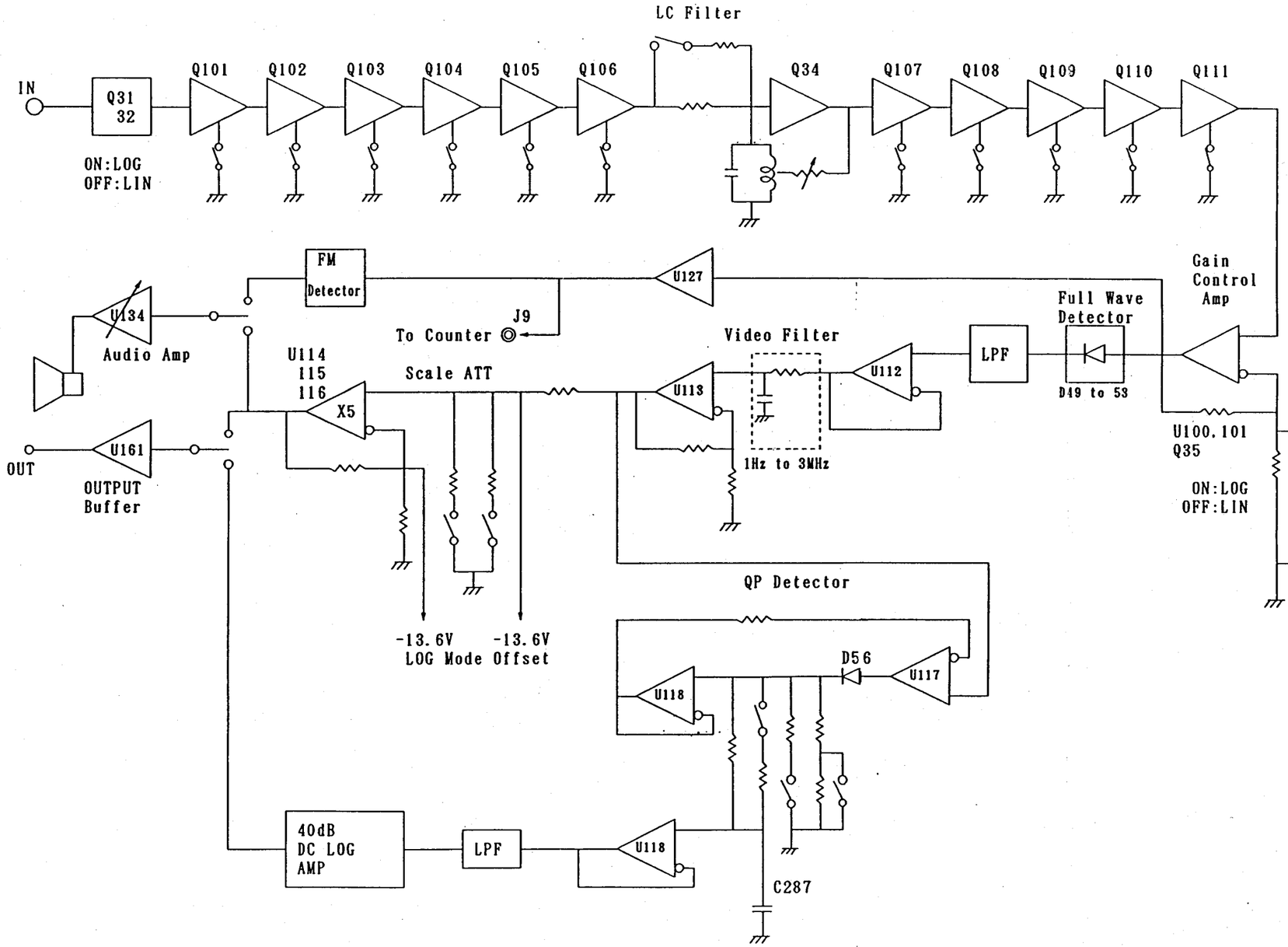


Figure 3.5-1 LOG AMP Block

3.5.2 Operation Description

The log amplifier block is designed as a true log system encompassing 10 double-gain amplifiers, U101 to U110.

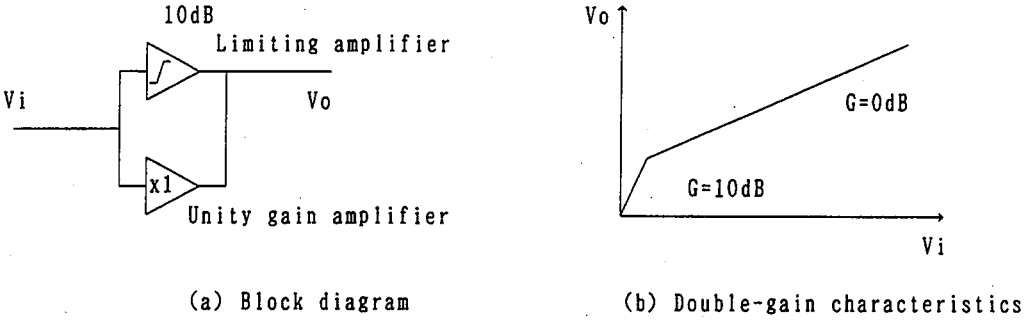


Figure 3.5-2 Double-gain Amplifier

As Figure 2 shows, a double-gain amplifier is a combination of two amplifiers, one with a 0dB gain and the other with a 10dB gain. Chaining 10 of such double-gain amplifiers together makes a log amplifier with a 0dB gain.

Because the dynamic range of the log amplifier is limited by amplification noise, the input signal is limited in frequency band by an LC filter and, further, noise figure is improved by the use of a preamplifier composed of Q31 and Q32 to widen the dynamic range.

The log-compressed signal is controlled by a gain adjustment amplifier consisting of Q100, Q101, and Q35 and detected by a full-wave detector consisting of Q49 through Q53.

The signal is then limited in band between 3MHz and 1Hz by a video filter circuit for input to a scale attenuator or QP circuit.

The scale attenuator selects the vertical axis setting (10dB, 5dB, 2dB, or 1dB/div).

The QP circuit detects the envelopes of the signal with a detector consisting of U117 U118, and D56 and a charge/discharge circuit consisting of R334 through R338 and C287.

The switch is set according to the set frequency to vary the charge/discharge time constant. The QP-detected signal passes through a low-pass filter and log-compressed by a 40dB DC log amplifier for output.

Signals controlled in the LOG, LIN, or QP Mode pass through the output buffer, U161, and output to the A/D block.

The audio FM detector, U128, detects FM signals following the switch selection of FM/ AM, which are then amplified by the audio amplifier, U134, for output to PHONE OUT.

3.6 A/D BLOCK AND RAMP GENERATOR BLOCK

3.6.1 Block Diagrams

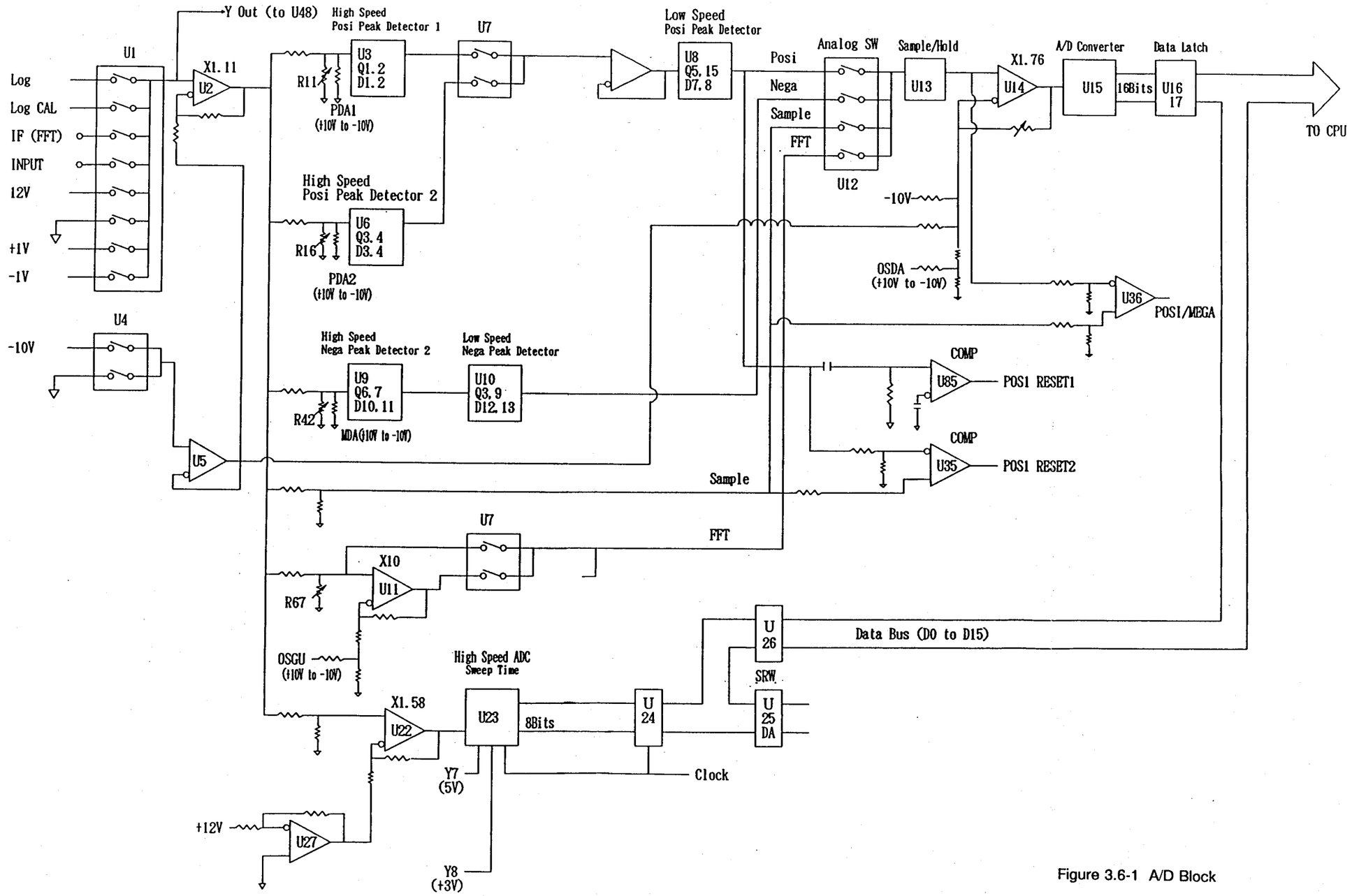


Figure 3.6-1 A/D Block

3.6.2 Operation Description

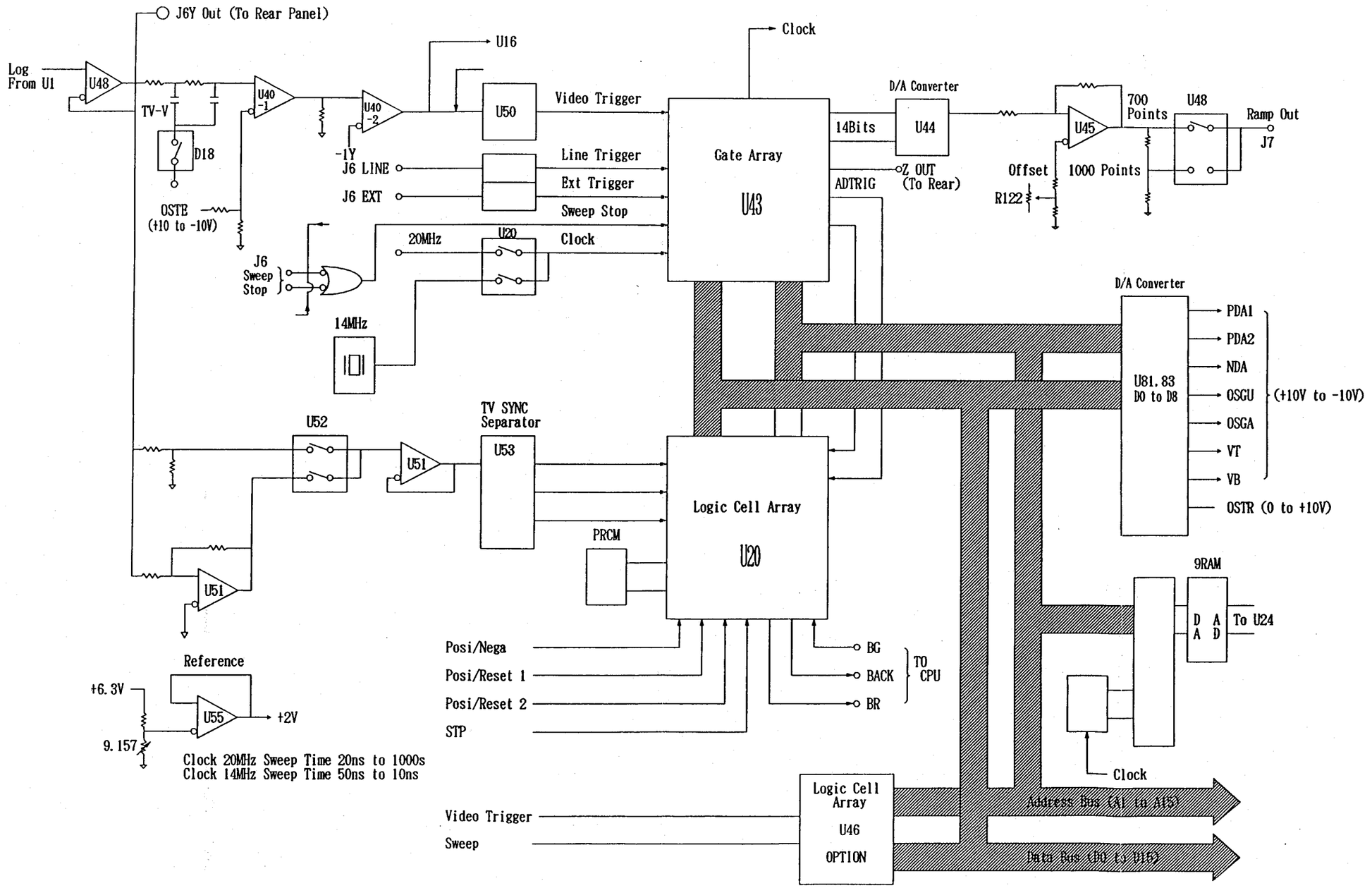


Figure 3.6-2 Ramp Generator Block

A/D conversion

Sweep time ≥ 20ms (normal speed)
The signal input from the log amplifier passes through a pair of high-speed positive peak detectors and a pair of low-speed negative peak detectors, a low-speed positive/negative peak detector, and a sample hold circuit before it is sent to the A/D converter.

Sweep time < 20ms (high speed)
The input signal goes through an 8-bit high-speed A/D converter consisting of U22 and U23, with the resultant digital data being sent to the CPU.

Digital IF
In Digital IF processing, the input signal (900Hz) is directed to the A/D converter without passing the log amplifier.

3.7 SYNTHESIZER BLOCK

3.7.1 Block Diagram

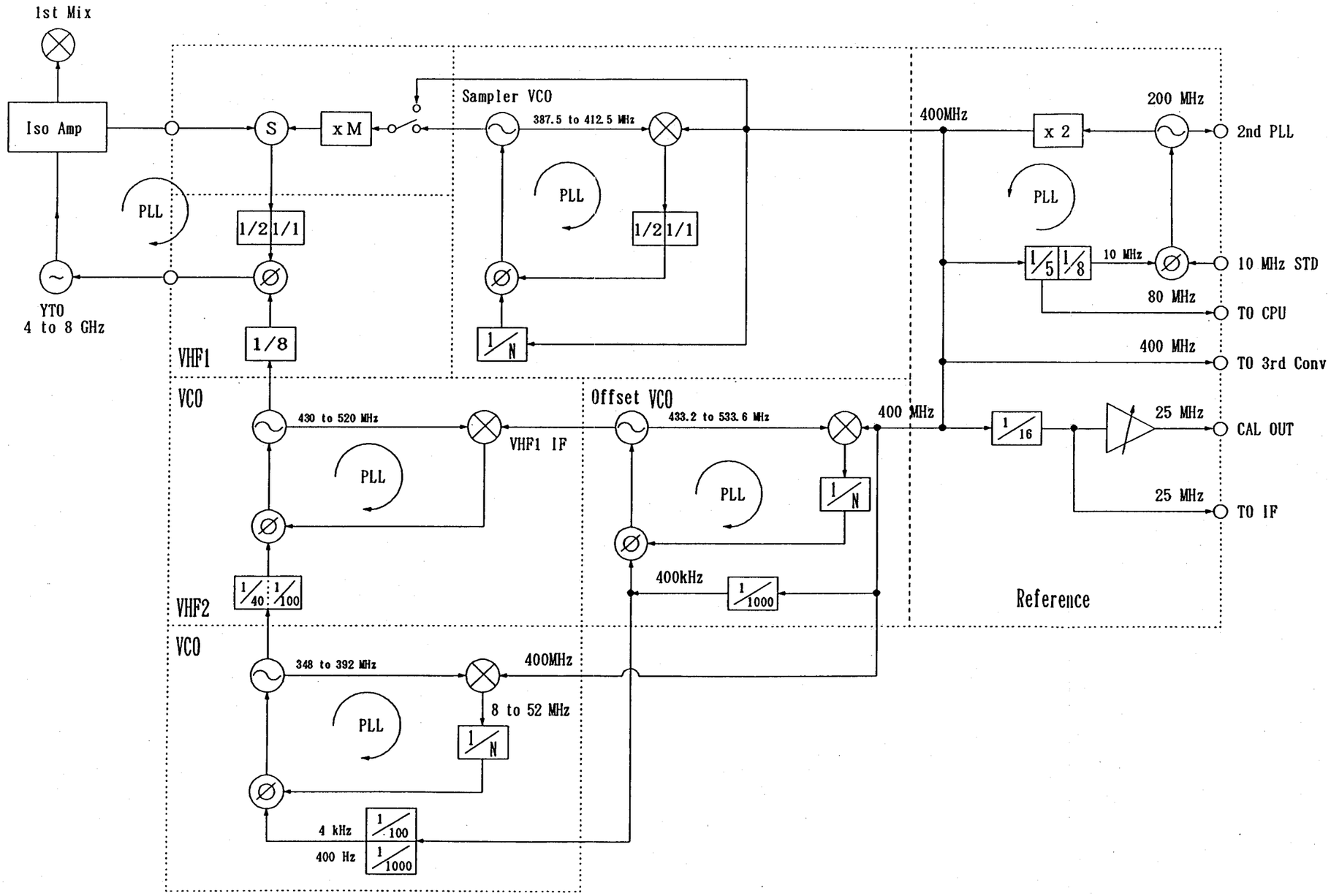


Figure 3.7-1 Synthe Block

3.7.2 YTO PLL

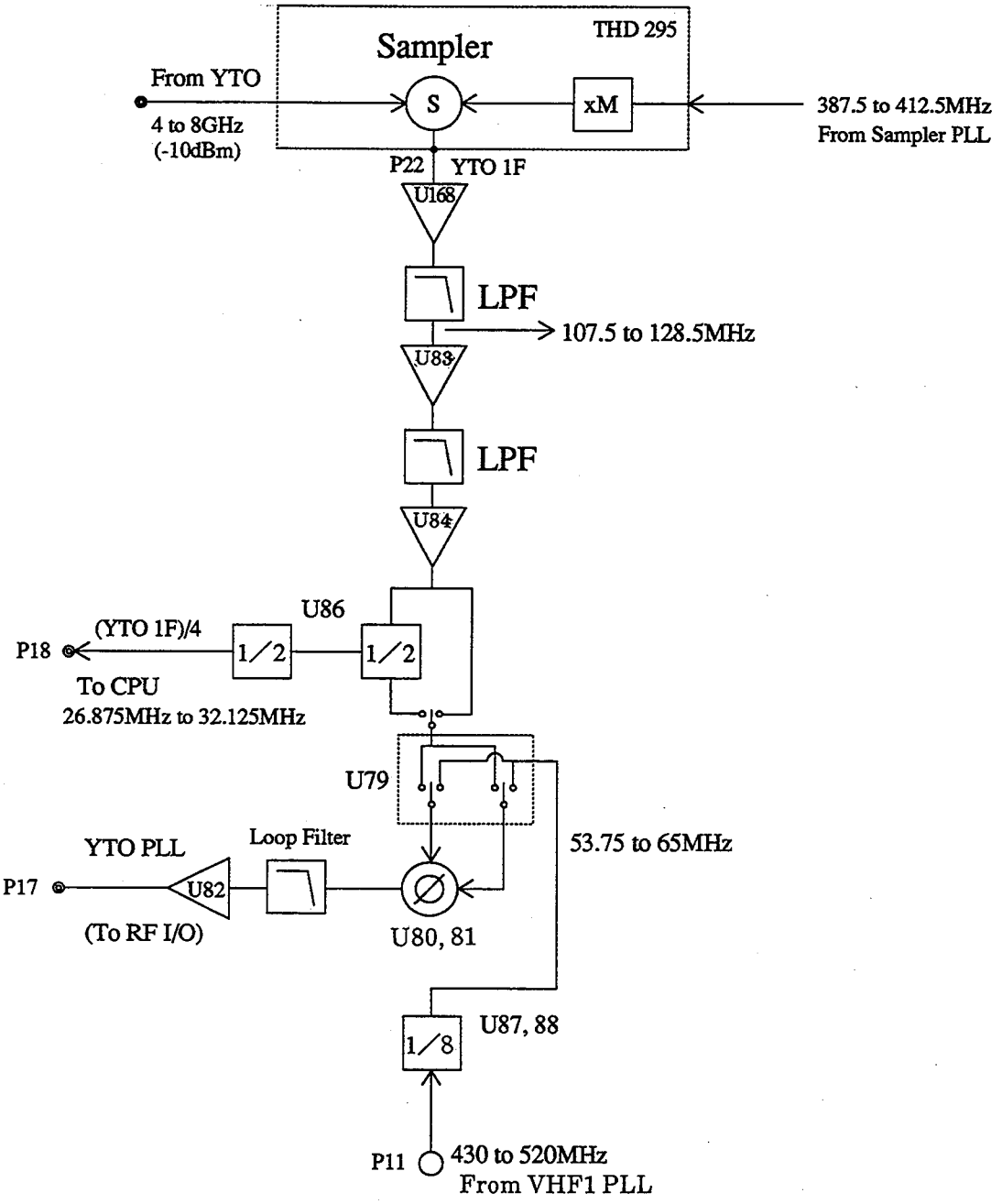


Figure 3.7-2 YTO PLL

In YTO PLL, a signal from Sampler, Synthe of Sampler PLL is generated to be pulse in SRD of Sampler (THD295), and YTO signal from Front End is sampled to generate YTO IF signal.
The phase comparison between YHF1 PLL and YTO IF generates PLL.
YTO IF signal, divided into quarter, is sent into a counter of CPU board to be used as a data receiving a frequency in the counter.

3.7.3 VHF1 PLL

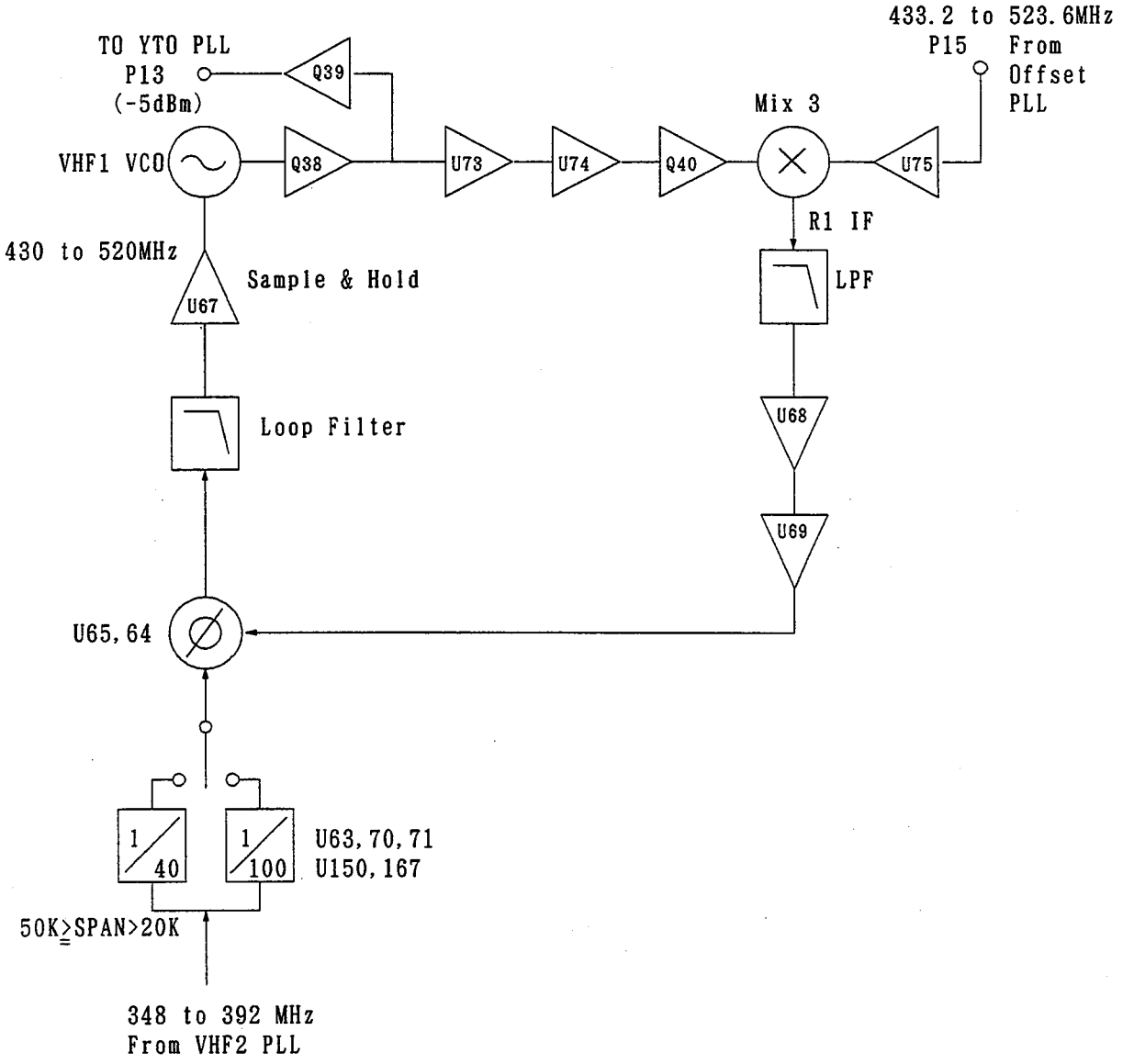


Figure 3.7-3 VHF1 PLL

The VHF1 PLL mixes the signals received from the VHF1 VCO and the offset PLL by using mixer 3, and compares the phase of the resultant VHF1 IF signal with that of the signal input from the VHF2 PLL as divided. Division by 40 is used only when the relation 50kHz ≥ span > 20kHz is true. Division by 100 is used for all other spans.

3.7.4 VHF2 PLL

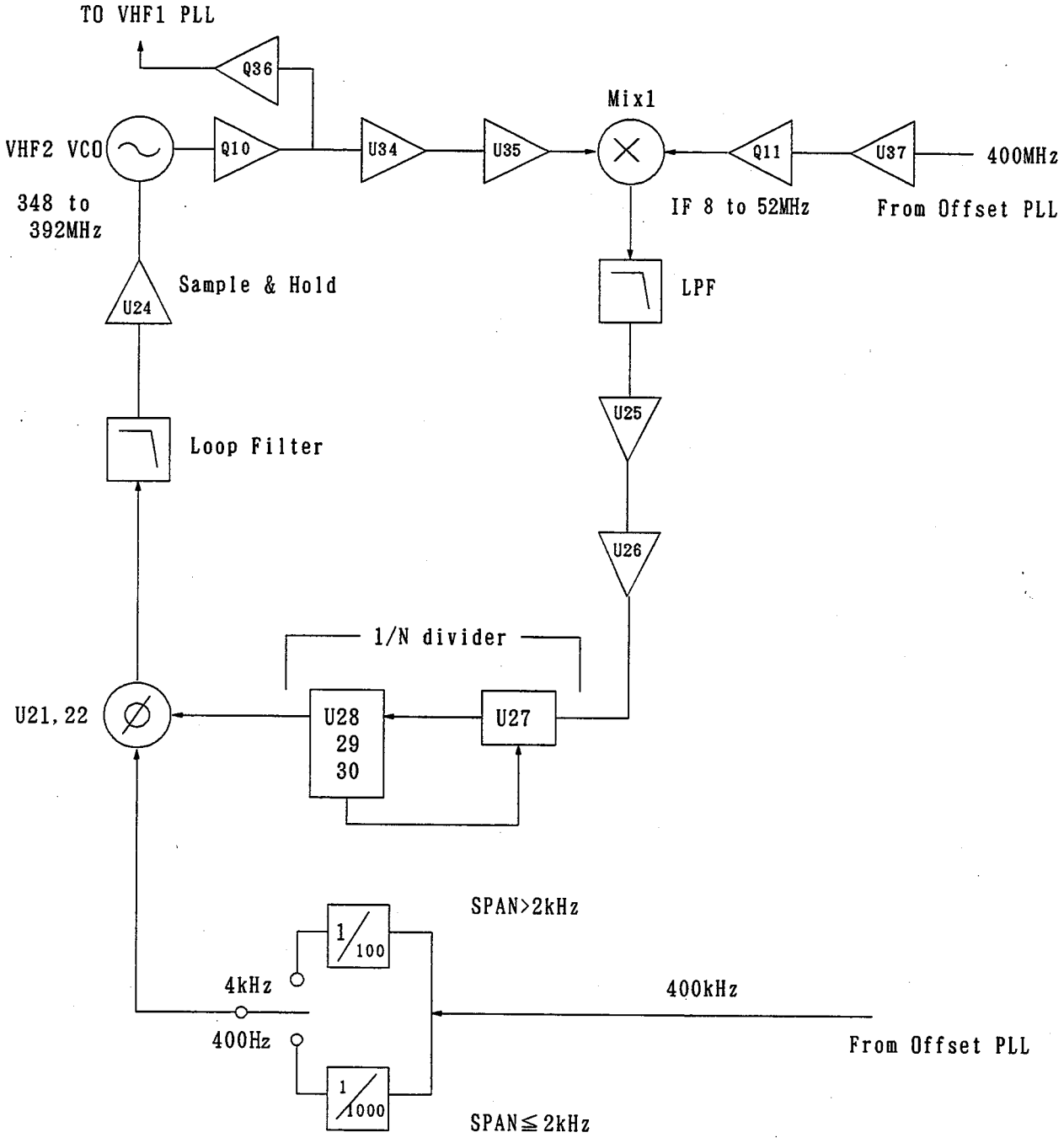


Figure 3.7-4 VHF2 PLL

The VHF2 PLL mixes the signals received from the VHF2 VCO and the offset VCO by using mixer 1, and compares the phase of the resultant VHF2 IF signal with that of the 400kHz signal received from the offset PLL.

3.7.5 Sampler PLL

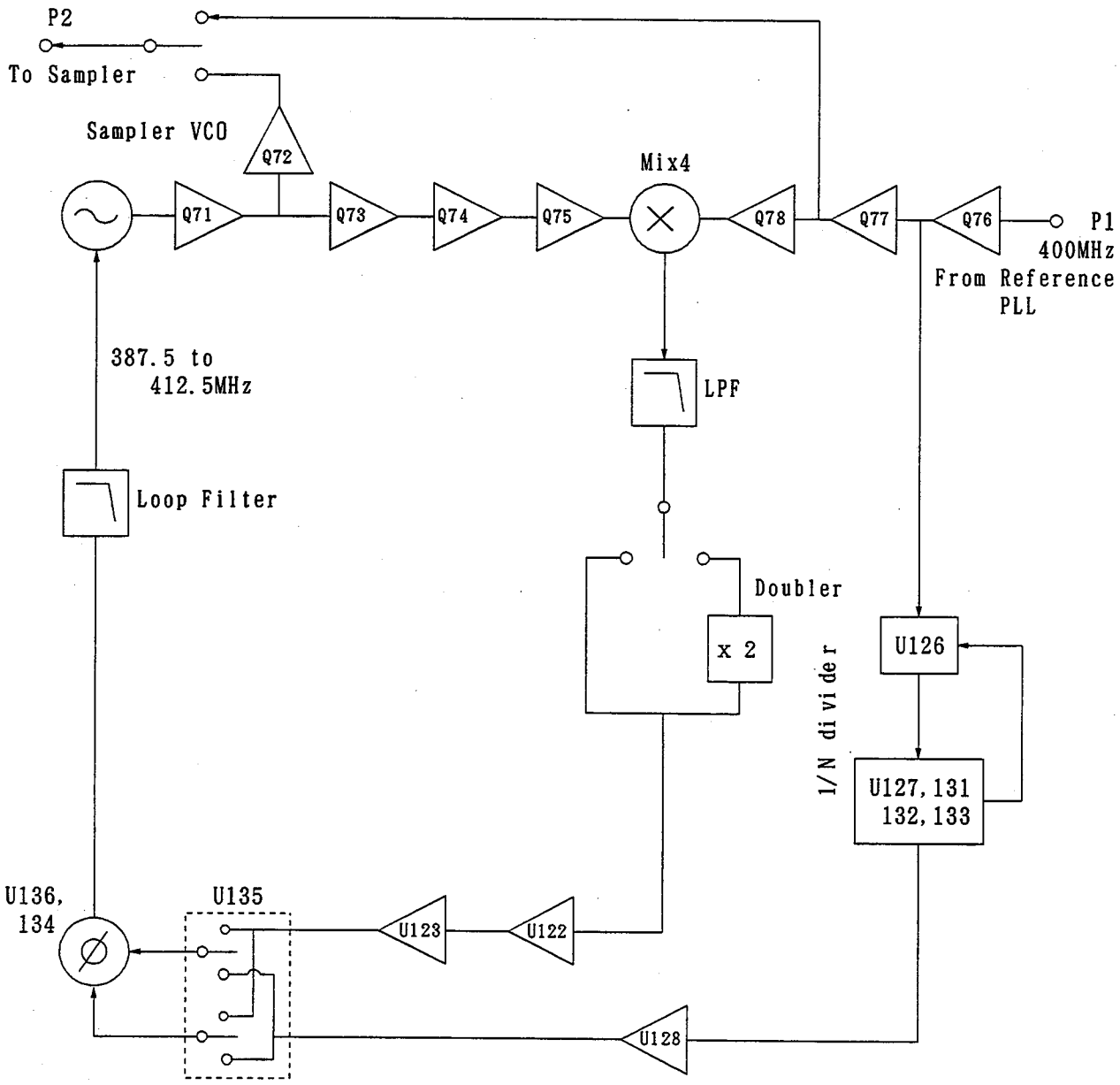


Figure 3.7-5 Sampler PLL

The sampler PLL mixes the signals received from the sampler VCO and the reference PLL by using mixer 4, and compares the phase of the resultant sampler IF signal with that of the 400MHz signal as divided by N.

3.7.6 Offset PLL

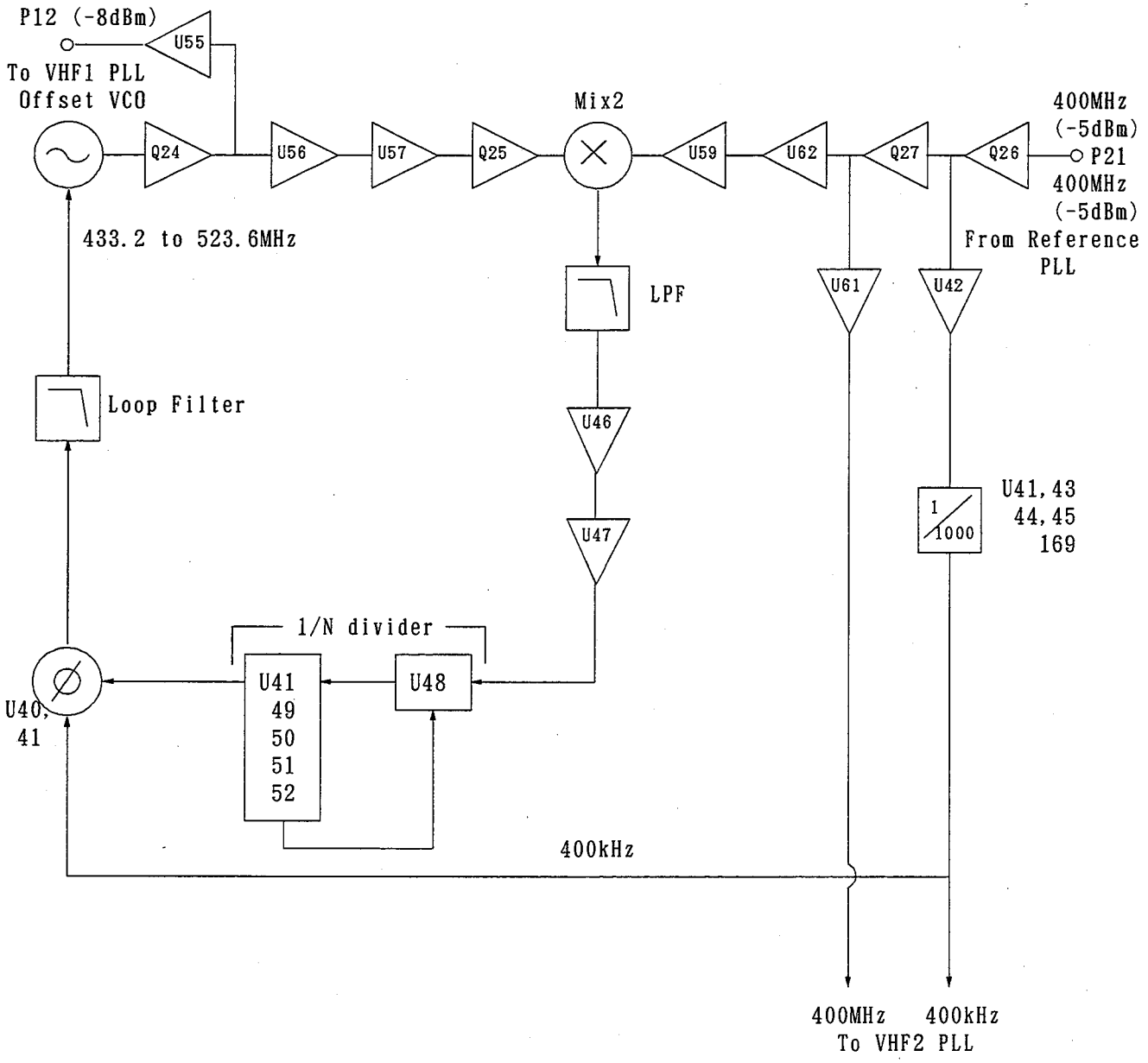


Figure 3.7-6 Offset PLL

The offset PLL mixes the 400MHz signals received from the offset VCO and the reference PLL by using mixer 2, and compares the phase of the resultant offset IF signal as divided by N with that of the 400MHz signal from the reference PLL as divided by 1,000.

The offset PLL operates in 400kHz steps (center frequency setting in 100kHz steps).

3.7.7 Reference PLL

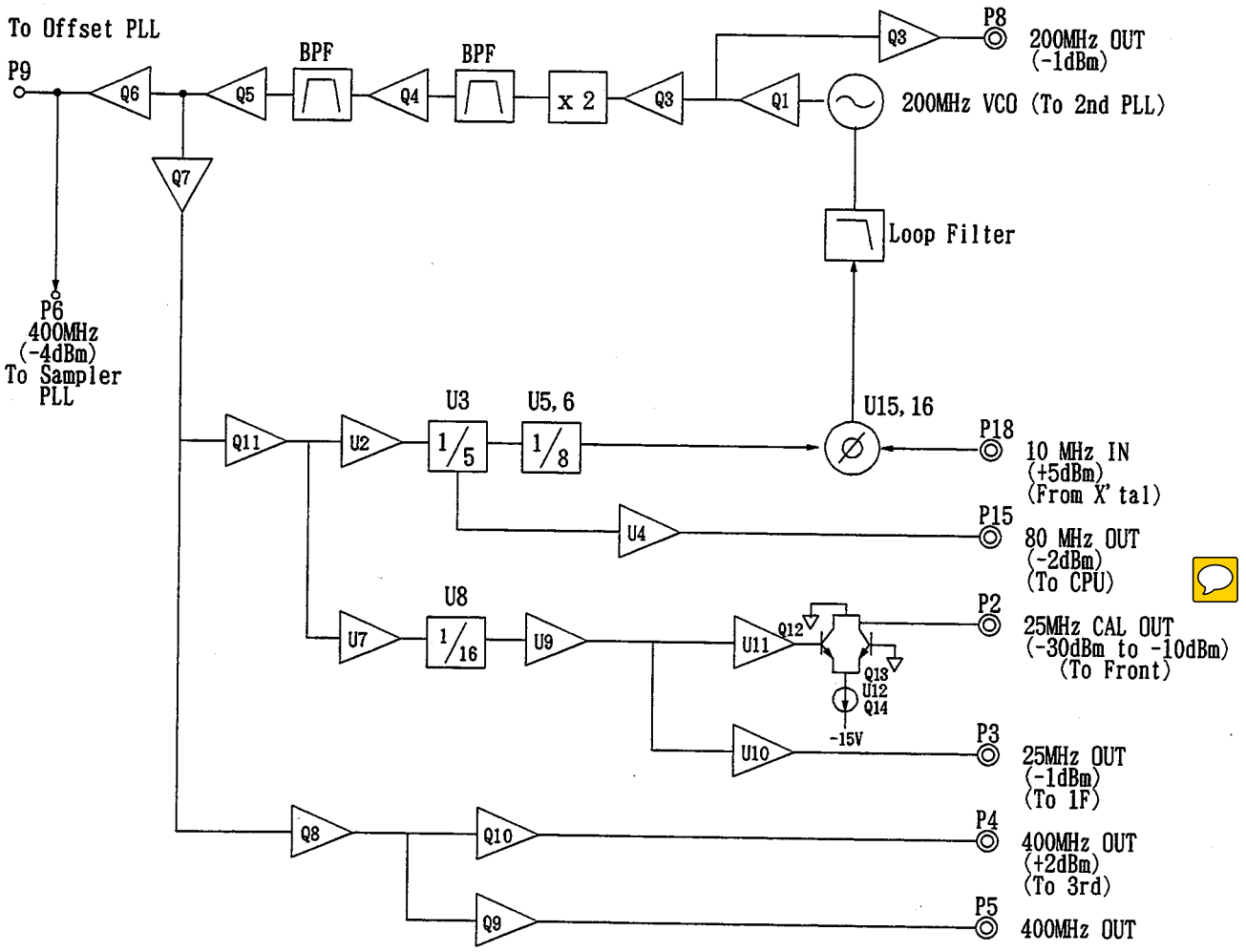


Figure 3.7-7 Reference PLL

The reference PLL establishes a frequency and Phase Noise basis for the R3265/3271. It boosts the 200MHz VCO output to 400MHz by using a doubler, then divides it by 40 to 10MHz, and compares its phase with that of the standard 10MHz.

3.7.8 Calibration Amplifier Operation Description

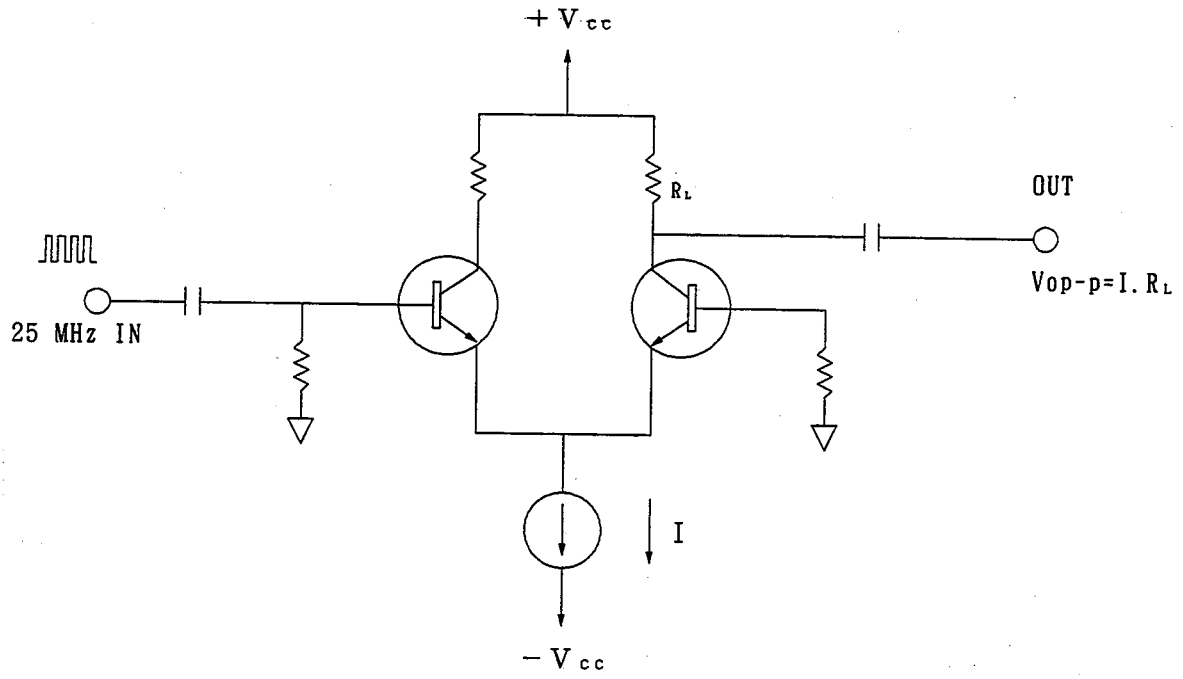


Figure 3.7-8 Differential Amplifier

The calibration amplifier is used to generate frequencies stabilized at 25MHz, which is obtained by dividing the 200MHz VCXO output that is phase-locked with an internal reference source by eight. Level stability is accomplished by saturating a differential amplifier as shown above.

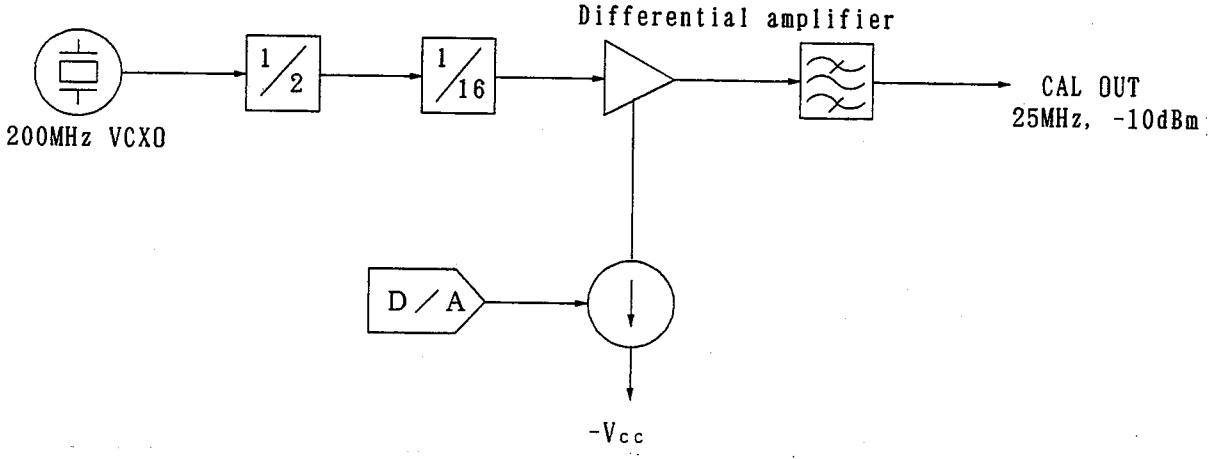


Figure 3.7-9 Differential Amplifier Control

The current I of the constant current source for the differential amplifier is regulated by the DA converter to vary the output in 0.5dB steps from −10dBm to −30dBm with high accuracy.

This signal is directed to the front panel BNC connector as the CAL OUT signal, which can be used for automatic level calibration purposes.

The output level available in the absence of automatic calibration is – 10dBm.

3.7.9 Span-Synthesizer Correspondence

Table 3.7-1 Span-Synthesizer Correspondence

<table>
<tr><th>Item / SPAN</th><th>YTO</th><th>Sampler PLL</th><th>VHF1 PLL</th><th>OFFSET PLL</th><th>VHF2 PLL</th><th>I/N ATT (RAMP)</th></tr>
<tr><td>SPAN > 500M</td><td>MAIN TUNE</td><td rowspan="9">LOCK</td><td rowspan="2">LOCK</td><td rowspan="9">* LOCK</td><td rowspan="3">LOCK</td><td></td></tr>
<tr><td>500M ≥ SPAN > 2M</td><td>SAMPLE & HOLD</td></tr>
<tr><td>2M ≥ SPAN > 400K</td><td rowspan="6">LOCK</td><td rowspan="2">SAMPLE & HOLD</td><td>1/1</td></tr>
<tr><td>400K ≥ SPAN > 50K</td><td>1/10</td></tr>
<tr><td>50K ≥ SPAN > 20K</td><td rowspan="4">LOCK</td><td>SAMPLE & HOLD 1/40</td><td rowspan="2">1/1</td></tr>
<tr><td>20K ≥ SPAN > 2K</td><td rowspan="3">SAMPLE & HOLD 1/100</td></tr>
<tr><td>2K ≥ SPAN > 200Hz</td><td>1/10</td></tr>
<tr><td>ZERO SPAN</td><td>LOCK</td><td></td></tr>
</table>

*LOCK: Locked off after being pulled in with a span higher than 500kHz but not exceeding 2MHz.

3.7.10 Typical Frequency Values of Synthesizers at Center Frequency Settings

Table 3.7-2 Typical Frequency Values of Synthesizer

CENTER f (MHz)	YTO (MHz)	YTO PLL (400M VCO)				Sampler PLL		
		POL U79	M	Sampler Vco (MHz)	VTO IF (MHz)	POL U135	XM	N
0	4231.4205	+	11	395.3488	117.4167	+	2	43
25	4256.4205	+	11	397.6744	117.9981	+	2	86
100	4331.4205	+	11	404.5854	118.5795	–	2	44
500	4731.4205	+	12	404.1666	118.5795	–	2	48
1000	5231.4205	–	13	393.2203	119.5560	+	1	59
2000	6231.4205	+	16	396.8253	117.7858	+	2	63
3000	7231.4205	–	18	395.1219	119.2253	+	2	41

CENTER f (MHz)	YTO (MHz)	VHF Synthe			
		Offset PLL	VHF1 PLL	VHF2 PLL	
		N1	R1 IF (MHz)	N2	NN2
0	4231.4205	183	3.533162	11670	116709
25	4256.4205	189	3.607581	9810	98104
100	4331.4205	195	3.682	7949	79499
500	4731.4205	195	3.682	7949	79499
1000	5231.4205	205	3.775627	5609	56093
2000	6231.4205	187	3.656603	8584	85849
3000	7231.4205	202	3.898487	2537	25378

* SPAN > 2K : Use N2.
* SPAN ≤ 2K : Use NN2.

3.8 TUNED SWEEP BLOCK

3.8.1 Block Diagram

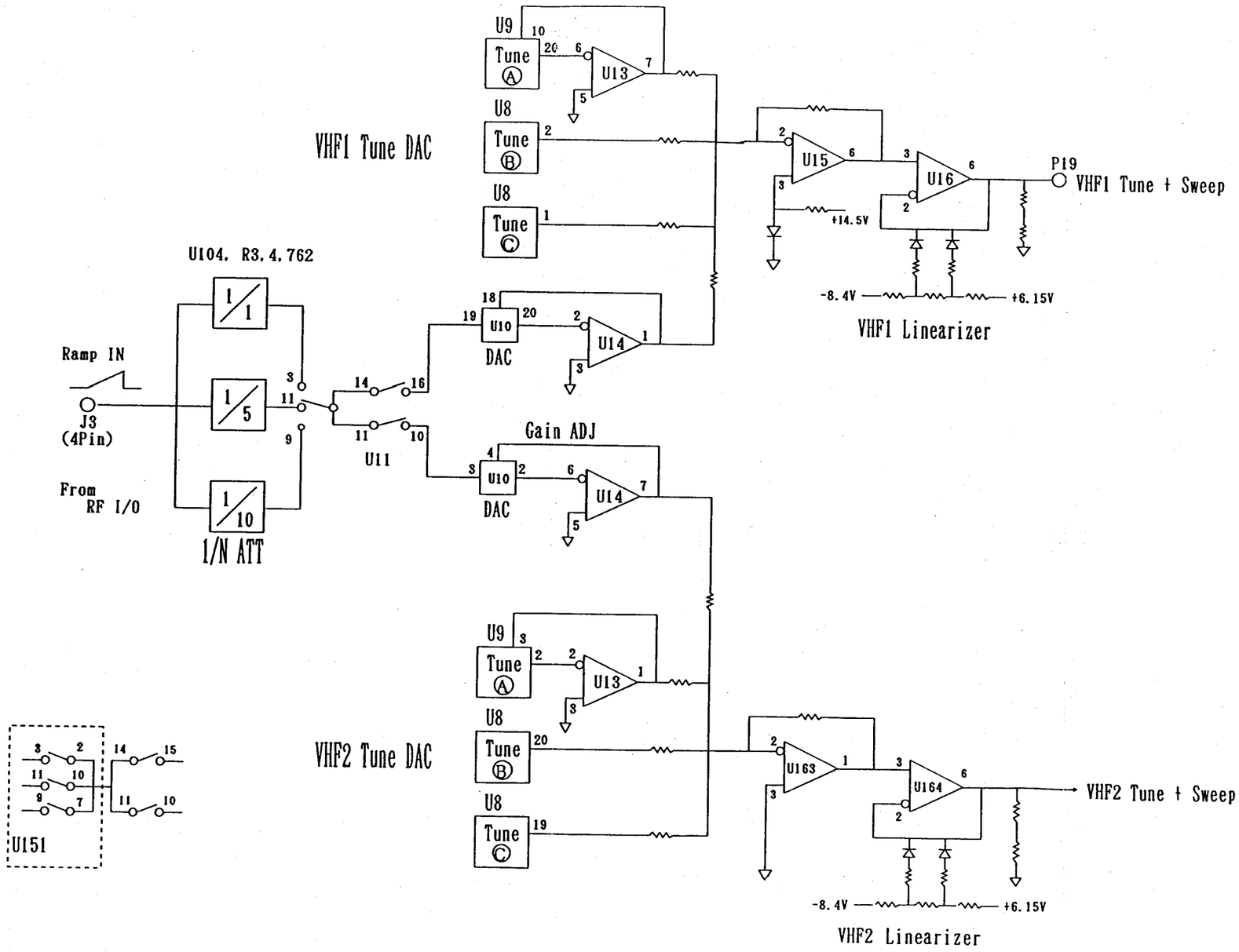


Figure 3.8-1 Tune Sweep Block

3.8.2 Operation Description

The ramp signal input from the RF I/O block is switched by U11, then attenuated to 1/N (attenuation to 1/5 is used only in special situations). The tuned sweep block also decides which is to be swept, VHF1 VCO or VHF2 VCO. The gain adjustment, VHF1 tuned DAC, and VHF2 tuned DAC are set by the CPU on the basis of calibration data stored in the EEPROM during adjustment. The gain-controlled ramp signal and tuned voltage are summed up by U15 (VHF1) and R169 (VHF2) before they pass through a linearlizer circuit to produce a tuned + ramp signal with corrected VCO linearity.

3.9 RF I/O BLOCK (YTO)

3.9.1 Block Diagram

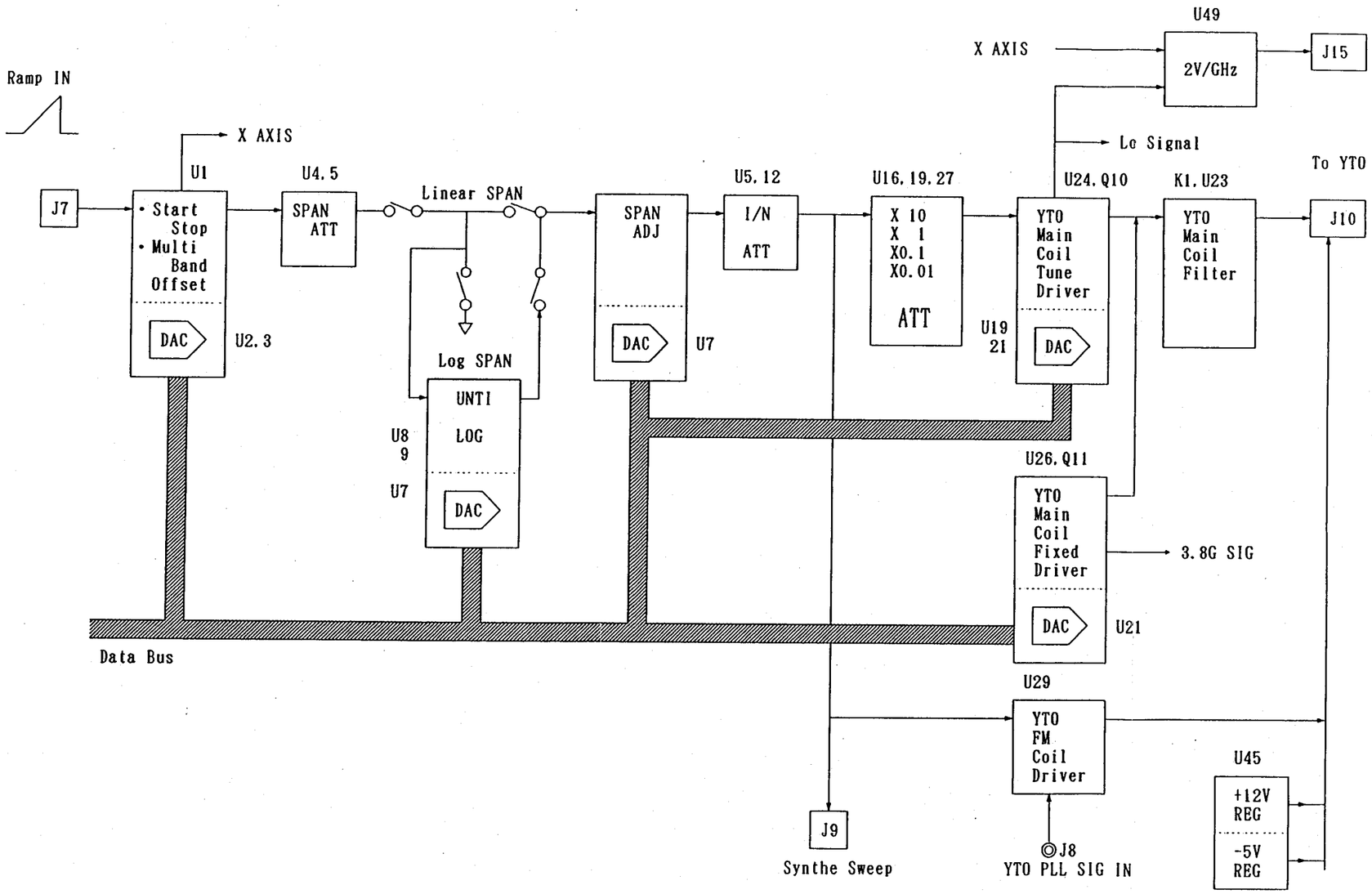


Figure 3.9-1 RF I/O Block Diagram (YTO)

3.9.2 Start and Multiband Offset DAC

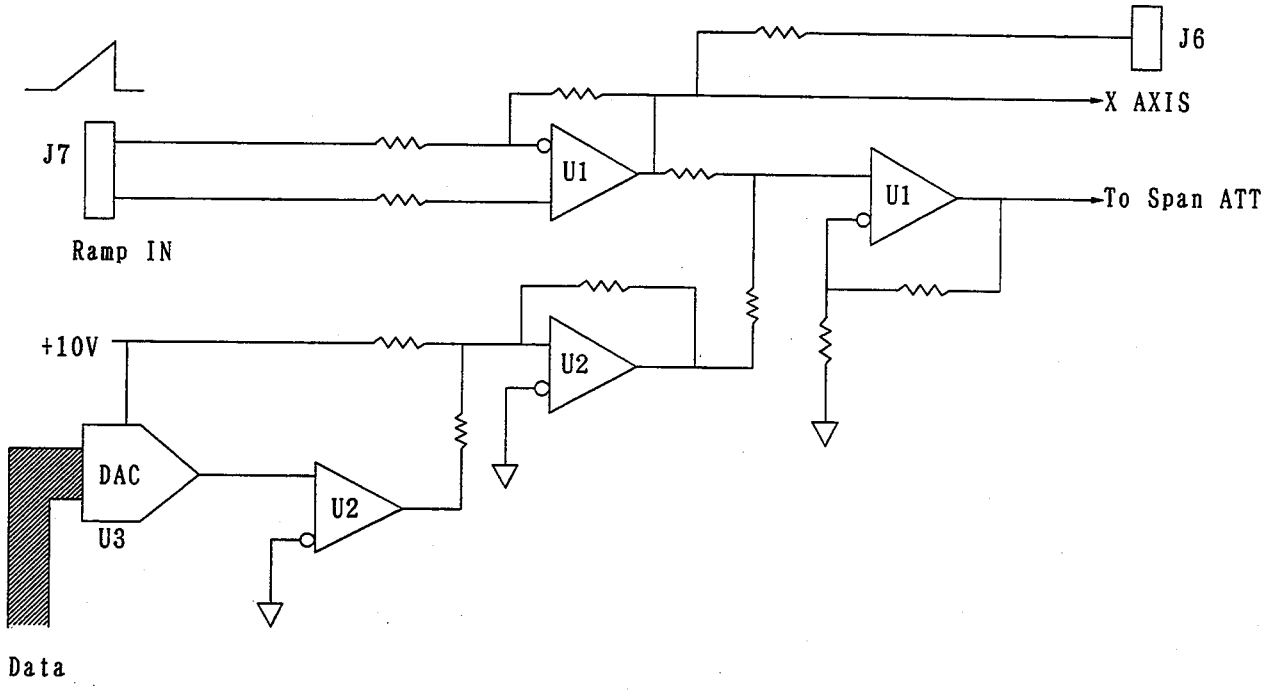
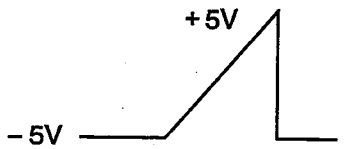


Figure 3.9-2 Start and Multiband Offset DAC

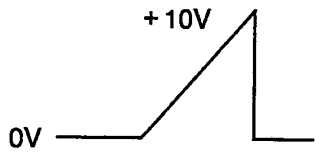
In the center span, start stop, and multiband modes, the start and multiband offset DA converter gives an offset to −5V to +5V ramp signals received from the log AD (BLS-017013)board.

Center Span



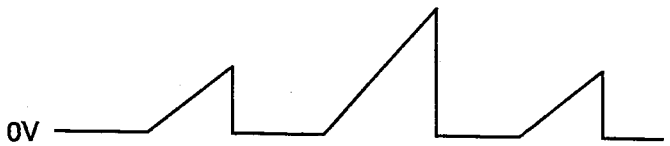
0V offset voltage

Start Stop



+5V offset voltage

Multi Band



The ramp voltage is adjusted to 0V at each band switching point.

3.9.3 Span Attenuator

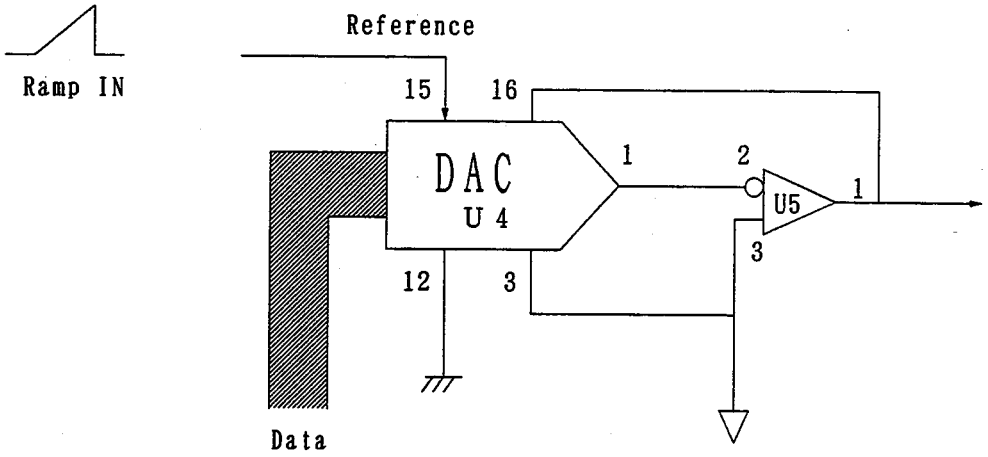


Figure 3.9-3 Span ATT

The ramp signal is input to a reference point of a DA converter of 12-bit multiplier type to determine the required rate of attenuation by varying the data with the span setting. The table below lists the rates of attenuation with varying span settings.

Span setting	Span ATT	Remarks
40GHz ≥ Span > 4GHz	4000/4095 to 401/4095	YTO Main Coil Sweep
4GHz ≥ Span > 400MHz		
400MHz ≥ Span > 40MHz		
40MHz ≥ Span > 10MHz	4000/4095 to 1000/4095	
10MHz ≥ Span > 2MHz	1000/4095 to 201/4095	YTO FM Coil Sweep
2MHz ≥ Span > 400kHz	2000/4095 to 401/4095	Synthe VCO Sweep
400kHz ≥ Span > 50kHz	4000/4095 to 501/4095	
50kHz ≥ Span > 20kHz	2000/4095 to 404/4095	
20kHz ≥ Span > 2kHz	2000/4095 to 201/4095	
2kHz ≥ Span > 200Hz	2000/4095 to 200/4095	

3.9.4 UNTI Log

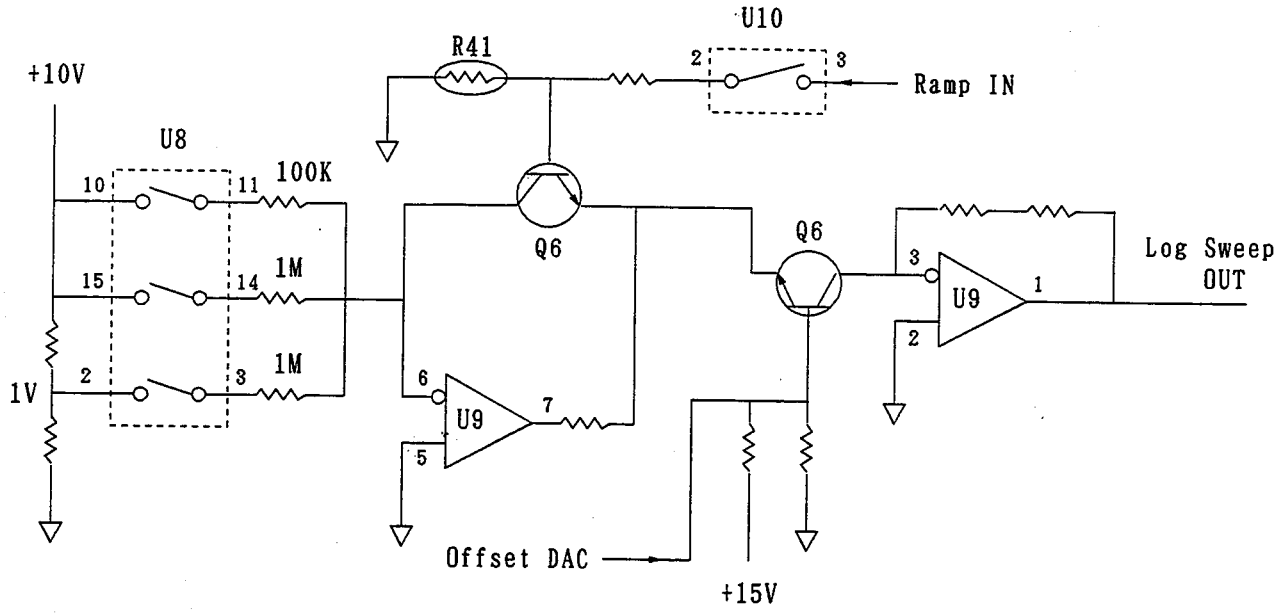
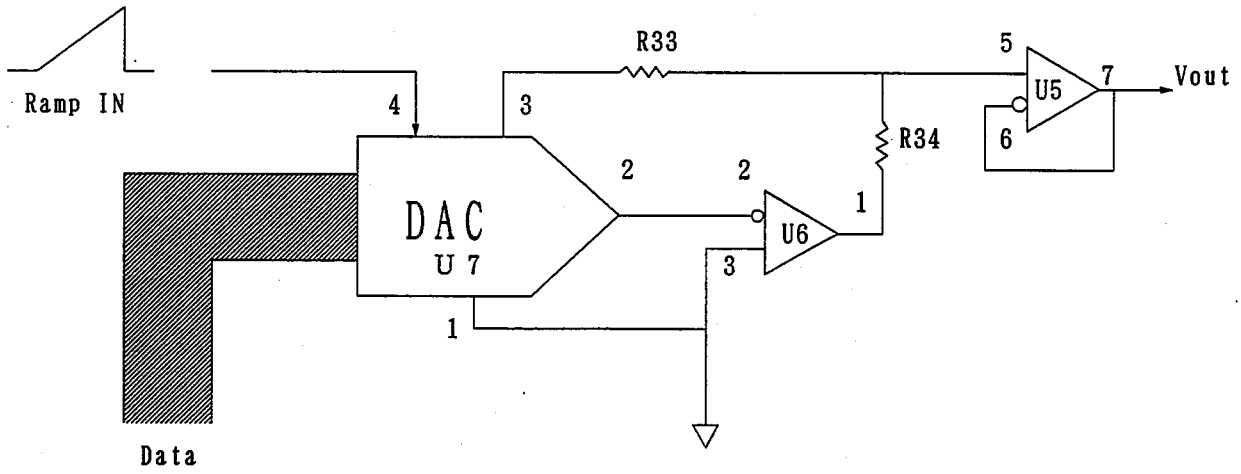


Figure 3.9-4 UNTI Log

With the log span setting, the input ramp signal passes through the UNTI log circuit to produce a log sweep signal. The UNTI log signal is derived from the V_{BE} -Ic characteristics of Q6. R41 is used for temperature compensation of these characteristics. R41 has a response of 3300 ppm/°C. With a log span setting of 3 decades, U8 (between 2 and 3) turns on, controlling the start and multiband DAC and the span attenuator to hold the input ramp signal between 0 and 7.3V. With a log span setting of 2 decades, U8 (between 14 and 15) turns on, regulating the input ramp signal between 0 and 4.9V; with a log span setting of 1 decade, U8 (between 10 and 11) turns on, allowing 0-2.4V ramp signals to be input to ramp IN.

3.9.5 Span Adjustment DAC and 1/N Attenuator

(1) Span adjustment DAC



$$Vout = Vin\left(1 - \left(1 + \frac{Data}{255}\right)\frac{R33}{R33+R34}\right)$$

Figure 3.9-5 Span ADJ DAC

Span adjustment is effected by the use of an 8-bit DA converter (U7). Span setting data is stored in EEPROM, and is updated every time the spans are reset.

(2) 1/N attenuator

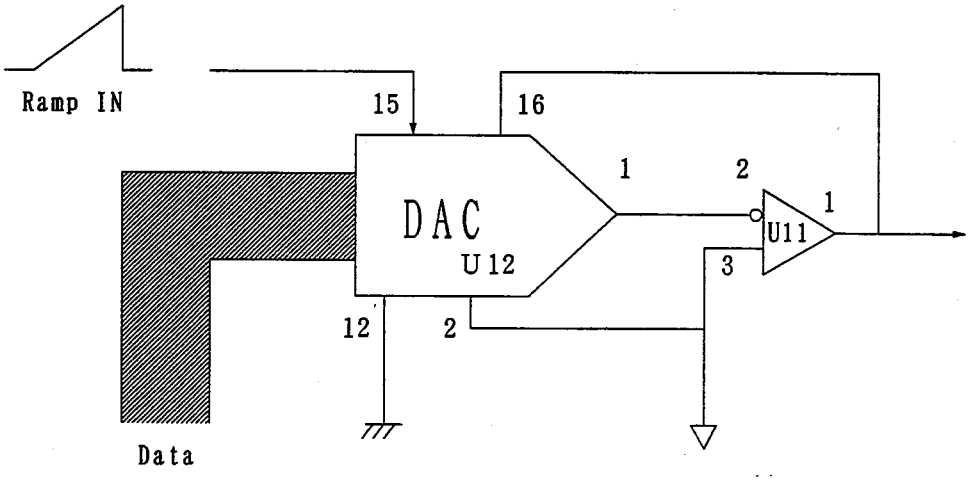


Figure 3.9-6 1/N ATT

The 1/N attenuator, similar in circuitry to the span attenuator, is a variable attenuator that uses a DA converter of multiplier type. When the harmonics mixer or external mixer is used, the 1/N attenuator attenuates the sweep ramp signal by the number of mixing degrees to 4,000/N (N being the number of mixing degrees).

3.9.6 YTO Main Coil Tuned DAC/Tuned Adjustment DAC

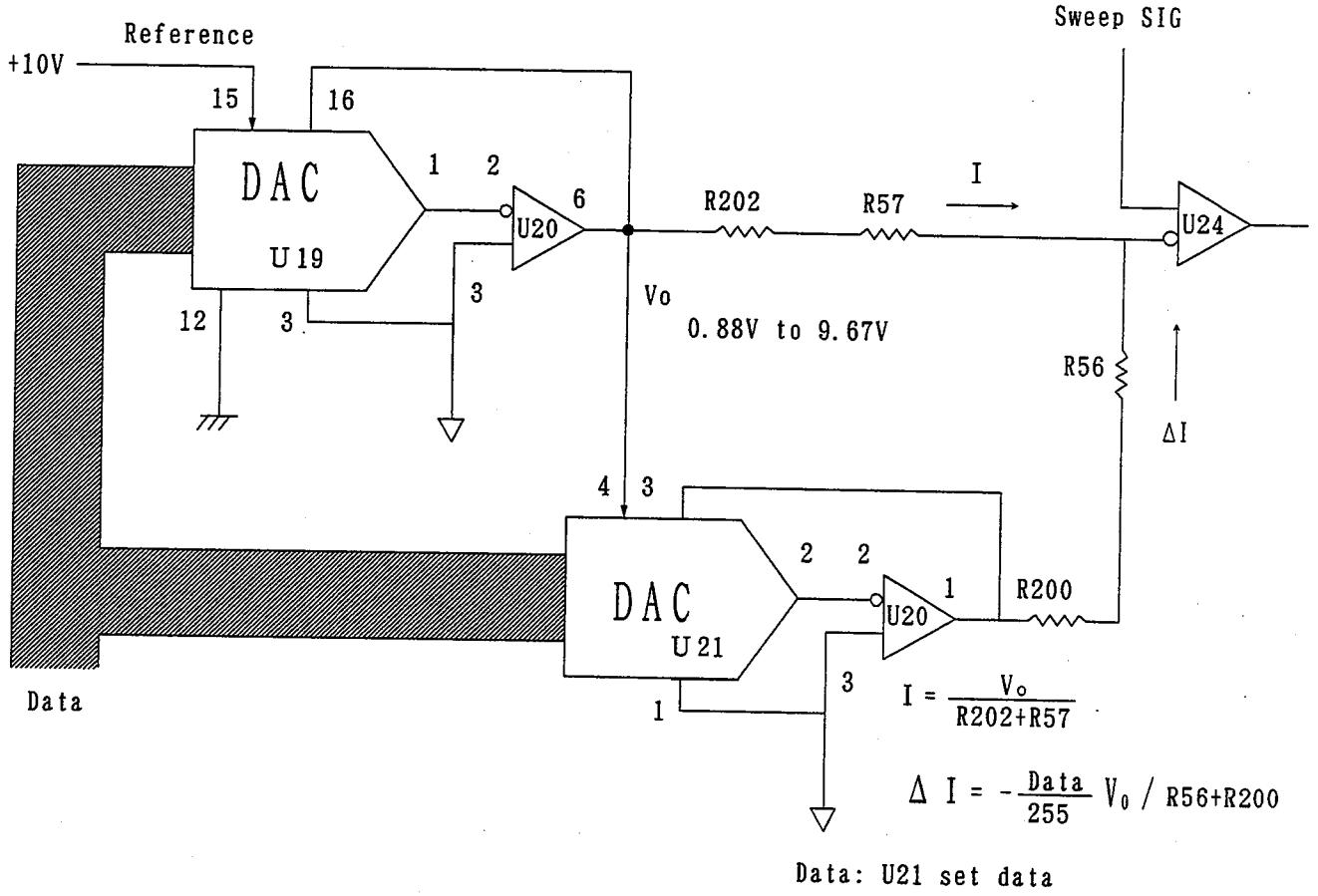


Figure 3.9-7 YTO Main Coil Tuned DAC/Tuned Adjustment DAC

U19 is a 12-bit DA converter that generates a YTO tuned voltage with resolutions of 1MHz x N. The output voltage is 0.88V for a 0MHz center frequency or 9.67V for a 3.6GHz center frequency.

U21 is a tuned adjustment DA converter. Its set data is adjusted for a YTO oscillation frequency of 7731.4MHz, with a center frequency setting of 3.5GHz. The adjustment data is stored in EEPROM in the CPU, and is read and reset when the power is turned on.

3.9.7 YTO Main Coil Tuned Driver/Main Coil Filter

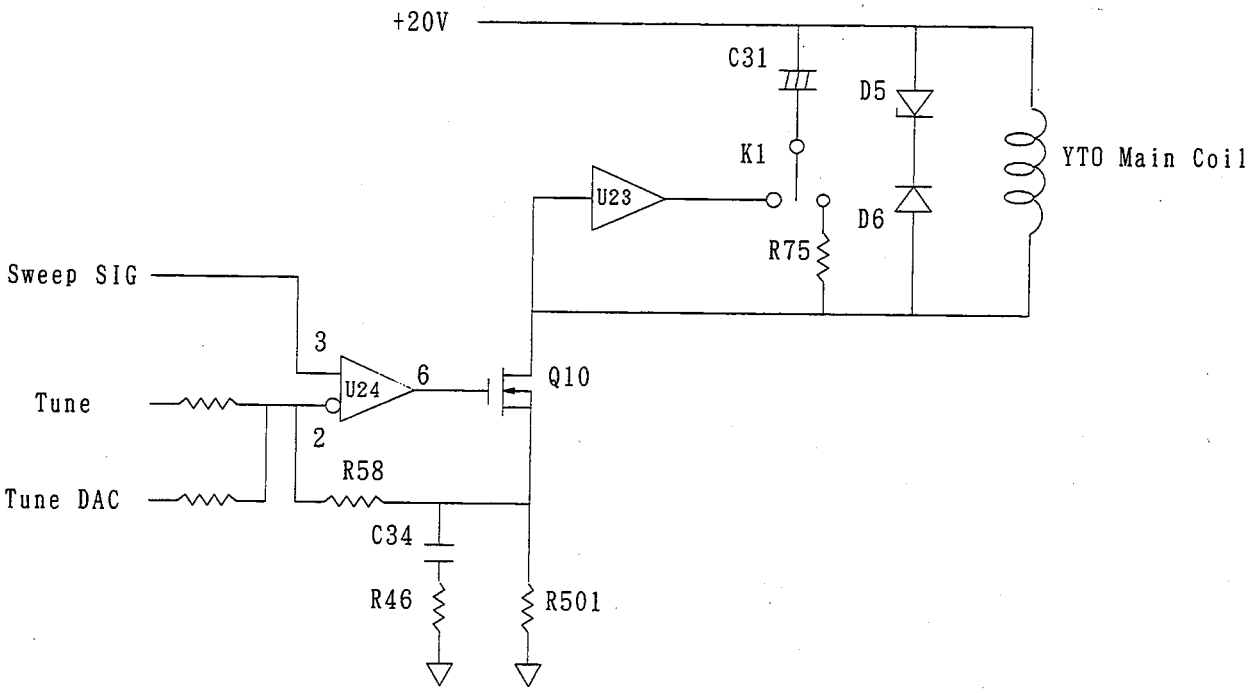


Figure 3.9-8 YTO Main Coil Tuned Driver/Main Coil Filter

The tuned voltage from the tuned DA converter and the sweep voltage (sweep SIG) from the span attenuator are converted to a current by a V-I conversion circuit consisting of V24 and Q10. The resultant current flows through the YTO main coil to determine the tuned frequency.

U23, C31, and R75 make up a YTO main filter. With a span setting of 10MHz or less, K1 is set to R75 and R75 and C31 are inserted in the YTO main coil to remove harmonics noise from it.

A charger circuit (U23) prevents a transient current from flowing through R and C to slow down the YTO response when this filter turns on. Consequently, transient current flow is suppressed when off to on transitions occur in the filter, thus speeding up the response time.

When the center frequency is varied by a wide margin (500MHz or more), the filter is turned off and charged with U23 to speed up the response before it is turned on again.

3.9.8 YTO Main Coil Fixed Driver/0GHz Adjustment DAC

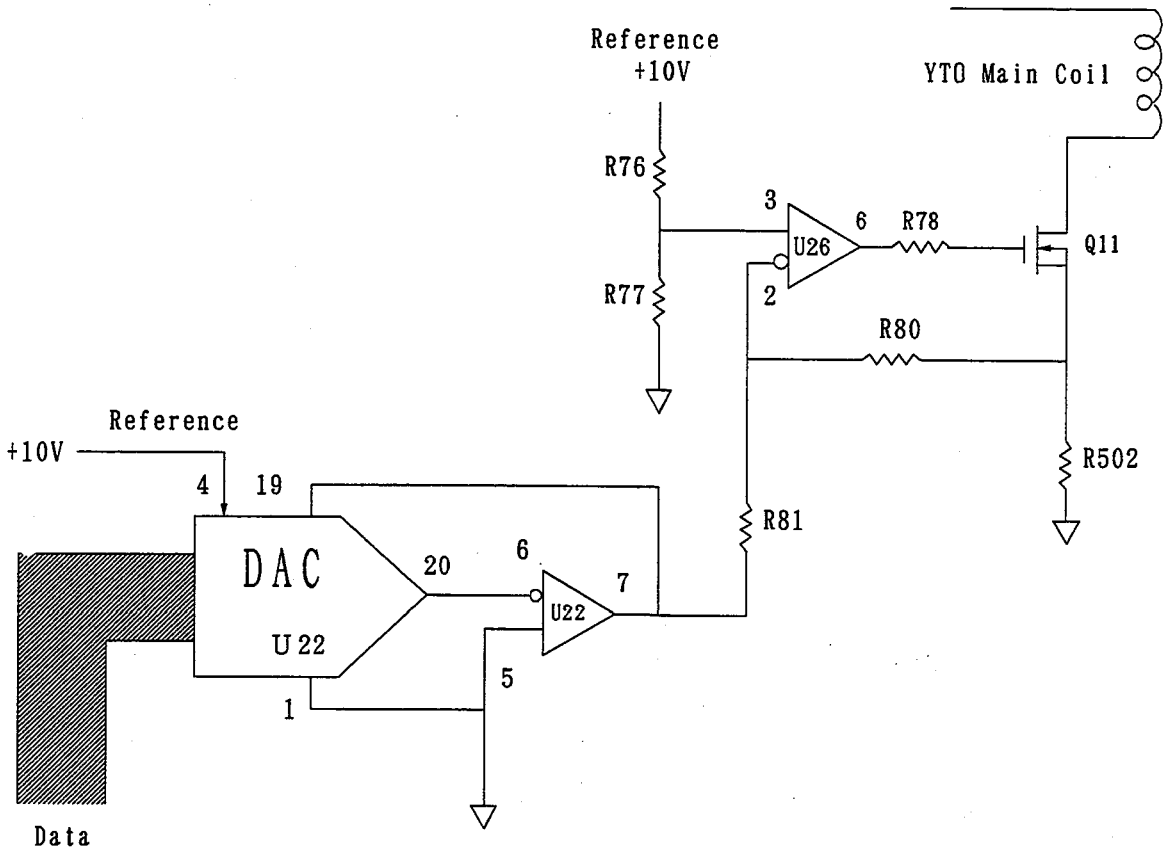


Figure 3.9-9 YTO Main Coil Fixed Driver/0GHz Adjustment DAC

A V-I conversion circuit consisting of V26 and Q11, the YTO coil fixed driver introduces a fixed tuned current through the YTO main coil.

Data set in the 0GHz adjustment DAC (U21, 22) is adjusted to set the YTO oscillation frequency to 4231.4MHz with a center frequency setting of 0MHz.

The adjustment data is stored in EEPROM in the CPU, and is read and reset when the power is turned on.

3.9.9 FM Coil Driver

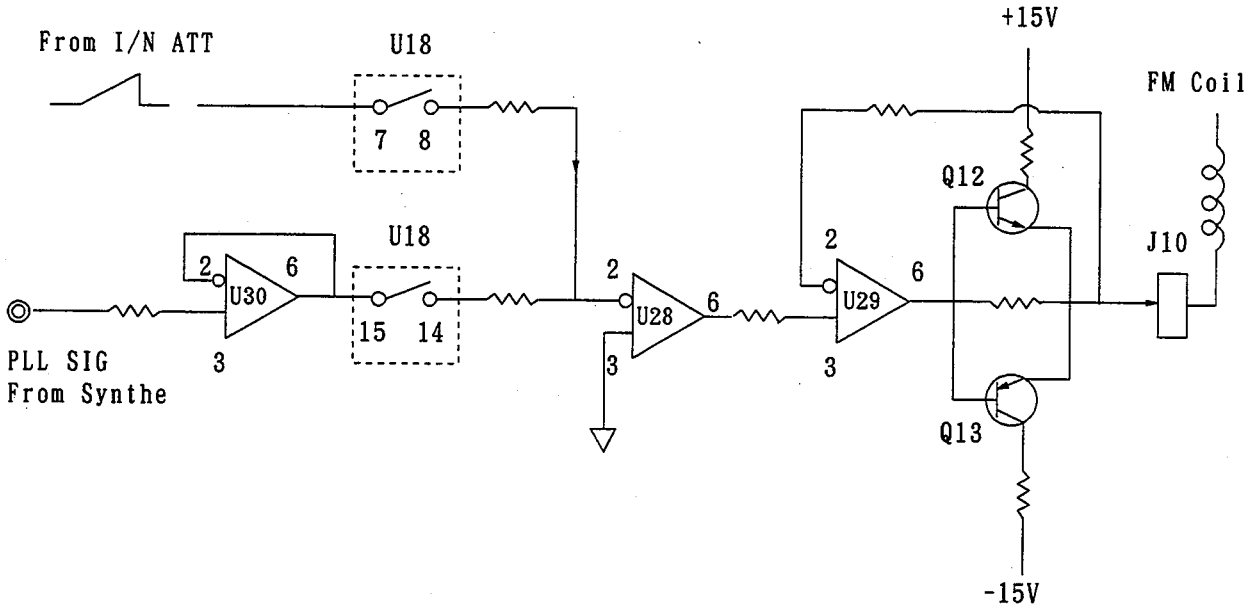


Figure 3.9-10 FM Coil Driver

YTO tuning by the FM coil is used for sweeping with a span setting of 10MHz or lower and for correcting YTO PLL error voltages.

The sweep signal passing through U18 (between 6 and 7) is added, at U28, to the YTO PLL error signal coming from U30, then led to the FM coil via a current buffer amplifier consisting of Q12 and Q13. The YTO FM coil has a current response of 300kHz/mA.

PLL error voltage addition takes place when the span setting is 500MHz or lower.

3.10 RF I/F BLOCK (YTF)

3.10.1 Block Diagram

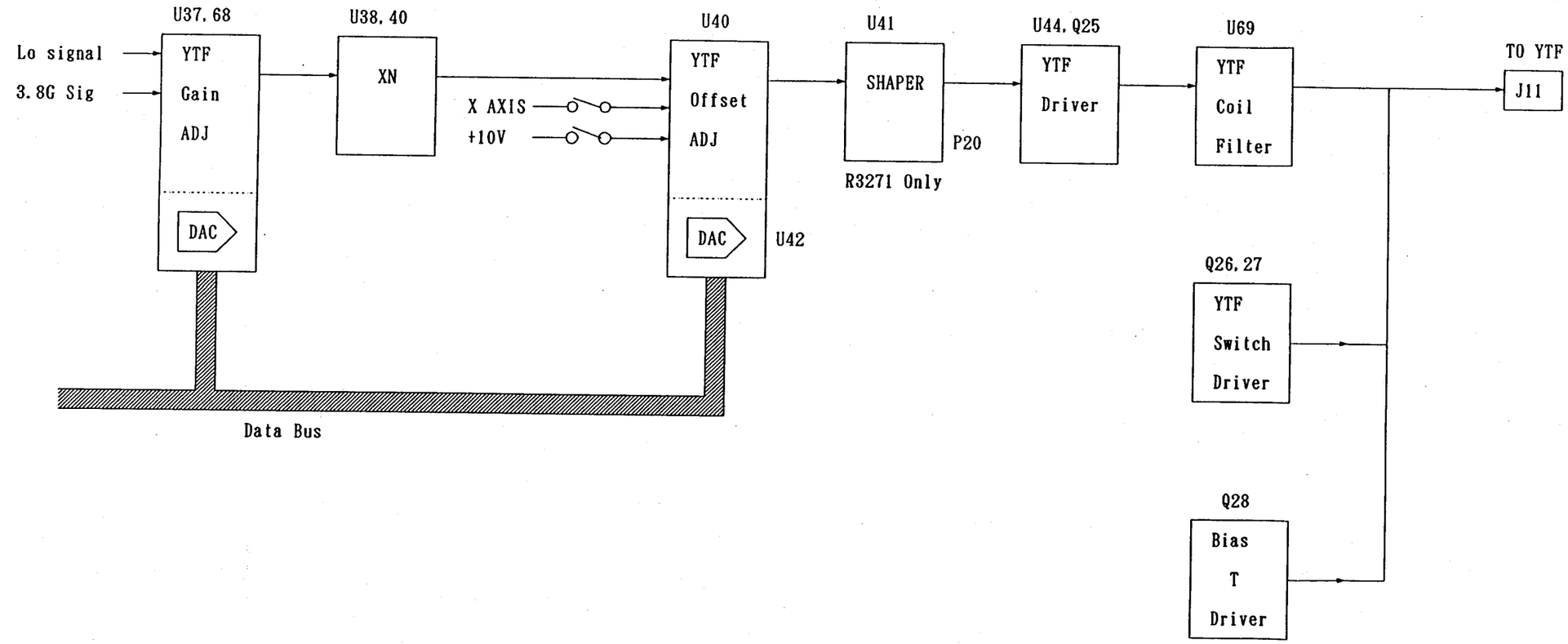


Figure 3.10-1 RF I/O Block Diagram (YTF)

3.10.2 Shaper, YTF Switch Driver, and Bias T Driver

(1) Shaper

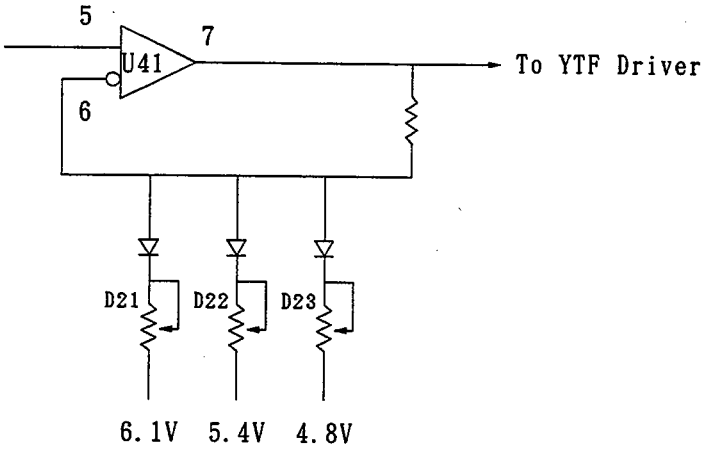


Figure 3.10-2 SHAPER

The shaper is a linearizer circuit that corrects YTF linearity when n to 4 (17 to 26.5GHz).

(2) YTF Switch Driver & Bias T Driver

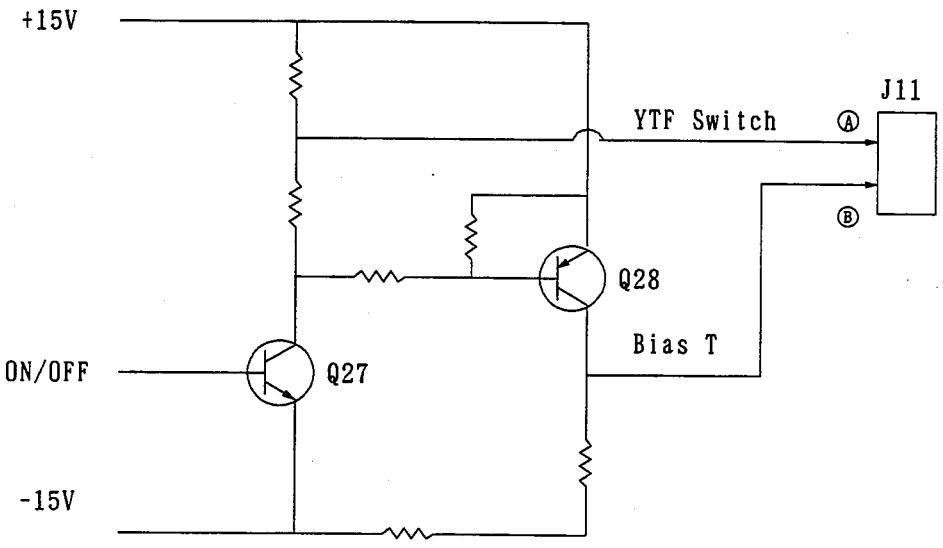


Figure 3.10-3 YTF Switch Driver & Bias T Driver

The YTF switch driver and the bias T driver control base band/high band switching in the YTF in the front end block.

		Q27	VTF Switch	Bias T
Base Band	0 to 3.6GHz	OFF	+15V	−15V
High Band	3.6GHz to	ON	−1VⒶ	+4VⒷ

*The YTF switch and the bias T generate ±15V with the J11 connector being removed.

3.11 RF I/O BLOCK (MIXING BIAS, ATTENUATOR DRIVER, FREQUENCY REFERENCE ADJUSTMENT)

3.11.1 Block Diagram

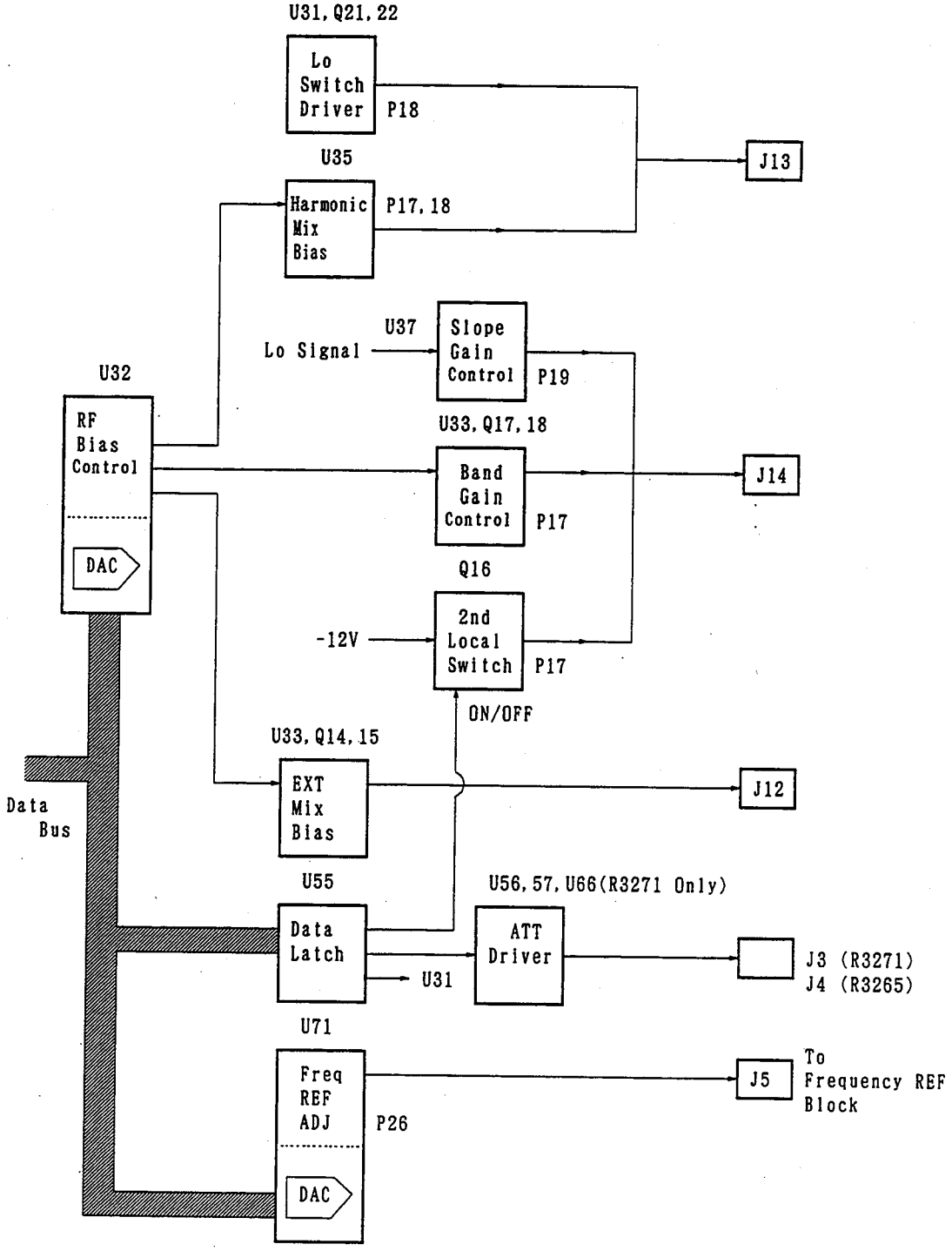


Figure 3.11-1 RF I/O Block Diagram

3.11.2 Local Switch Driver and Harmonic Mixing Bias

(1) Local Switch Drive

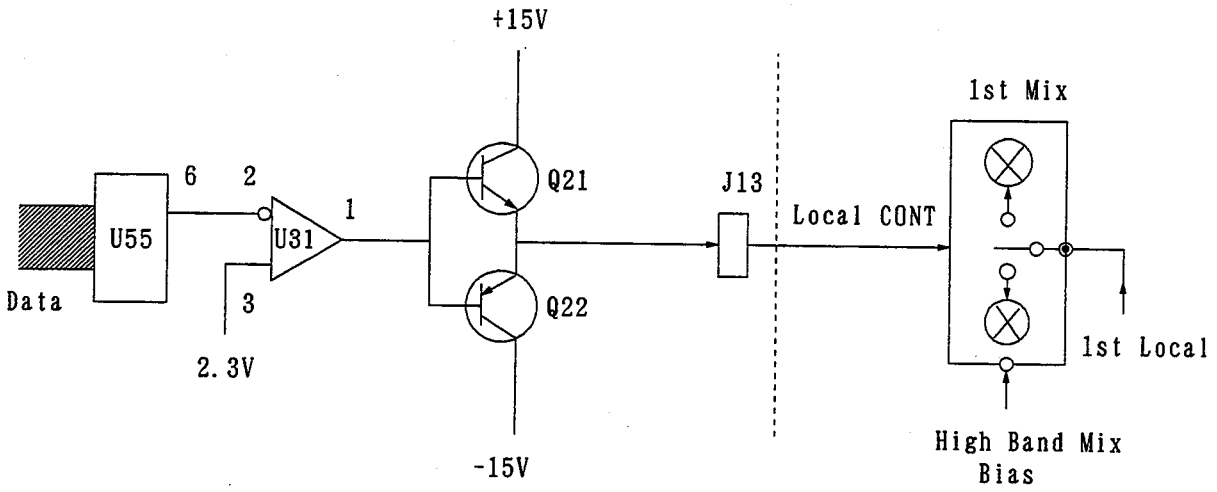


Figure 3.11-2 Local Switch Drive

The local switch driver selects the local signal to the first mixer in the front end block between the base band and high band.

(2) Harmonic Mixing Bias

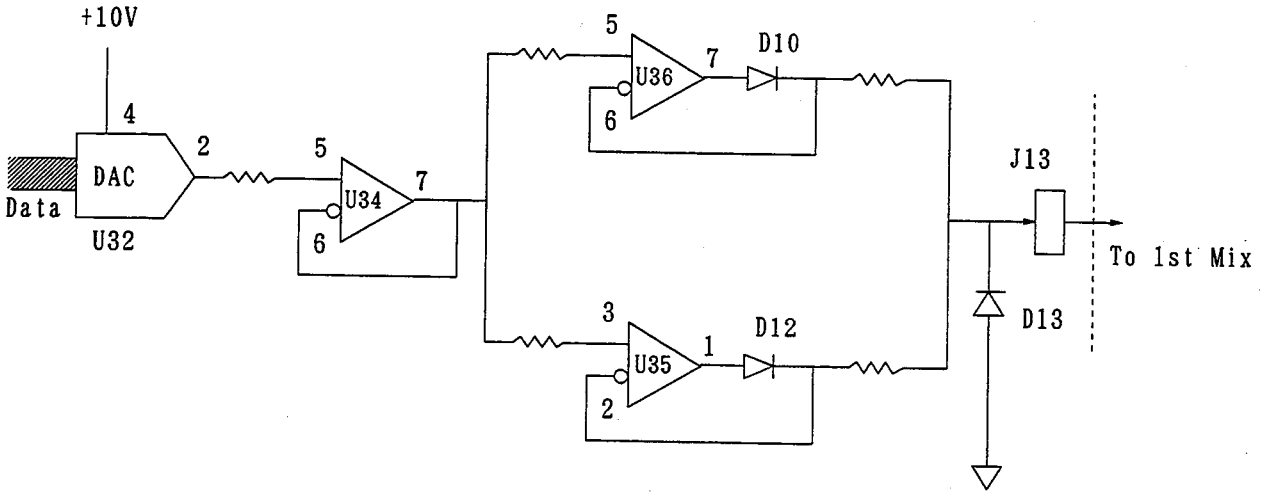


Figure 3.11-3 Harmonic Mixing Bias

The harmonic mixing bias uses a DA converter (U32) to provide a mixing bias for the high band setting. The mixing bias is selectable using the number of degrees of the local signal. The mixing bias is stored in EEPROM in the CPU and is reset every time the band selection is switched. Only the R3271 has a mixing bias.

3.11.3 Slope Gain Control and Band Gain Control

(1) Slope Gain Control

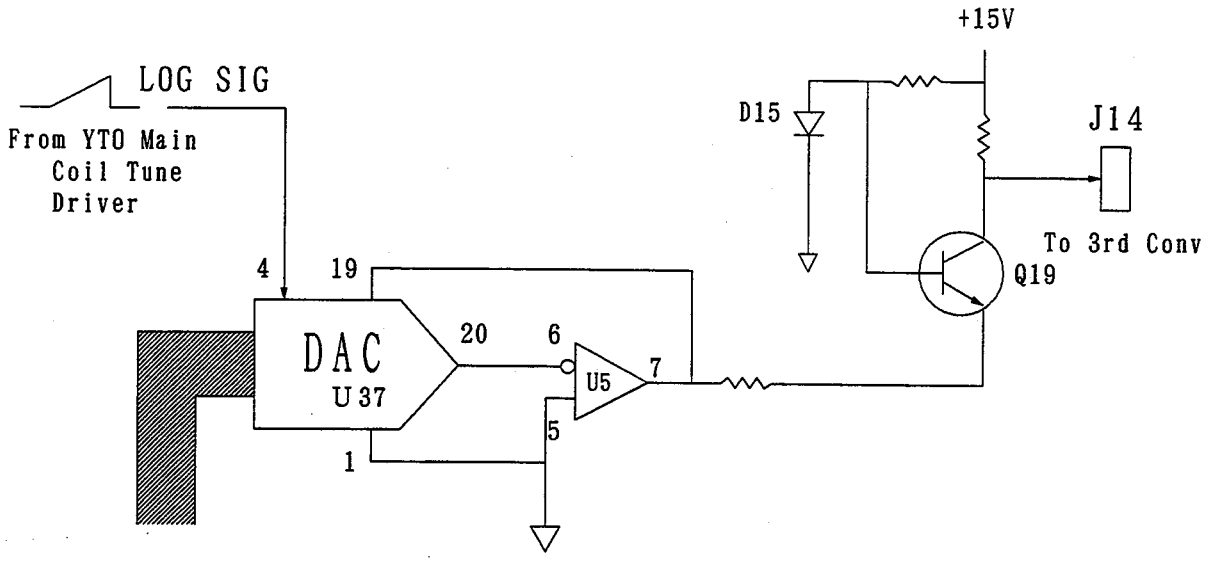


Figure 3.11-4 Slope Gain Control

The slope gain control uses a DA converter (U37) and Q19 to correct system frequency characteristics. The corrected value is stored in EEPROM in the CPU, and is called every time the center frequency or span is set, to control the slope gain amplifier in the third converter block for frequency characteristics correction. D15 is used for V_{BE} temperature compensation of Q19.

(2) Band Gain Control

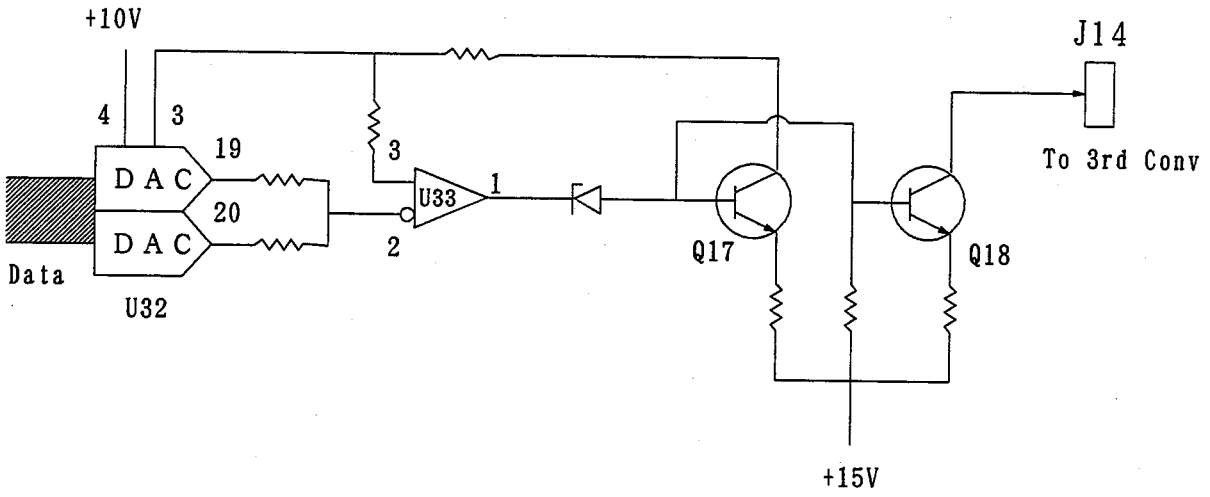


Figure 3.11-5 Band Gain Control

The band gain control uses a DA converter (U32, with four built-in DA converters), U33, Q17, and Q18 to correct the band-dependent conversion loss in the first mixer. The corrected values are stored in EEPROM in the CPU, and is called every time the band selection is switched, to control the band gain amplifier in the third converter block.

3.11.4 Second Local Switch and Attenuator Driver

(1) Second local switch

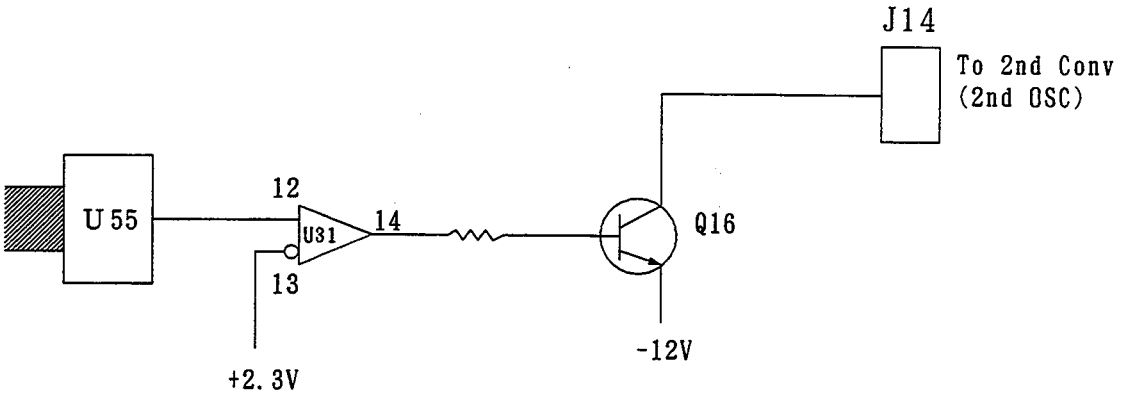


Figure 3.11-6 2nd Local Switch

The second local switch controls the second oscillator power supply (−12V). It turns on (to supply −12V) only when the base band (0 to 3.6GHz) is selected.

(2) Attenuator driver

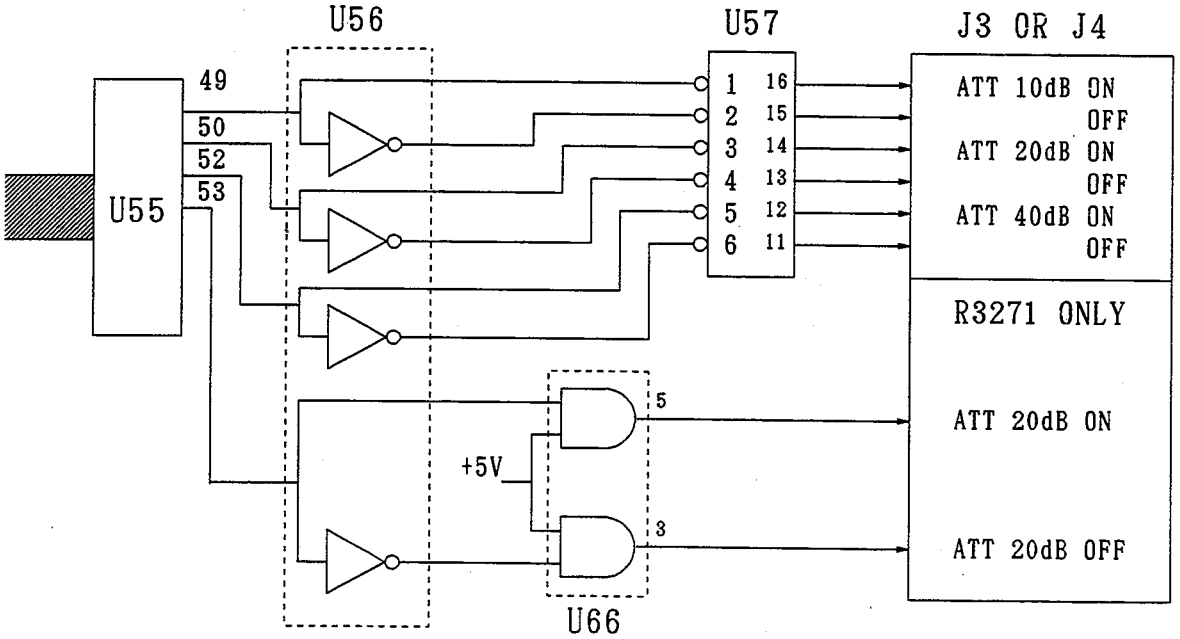


Figure 3.11-7 ATT Driver

The RF attenuator driver differs in its configuration between the R3265 and the R3271.
The RF attenuator in the R3265 is composed of three sections, 10dB, 20dB, and 40dB.
The RF attenuator in the R3271 has U36 added, because it is composed of four sections, 10dB, 20dB, 20dB, and 20dB.

3.11.5 Frequency Reference Adjustment DAC

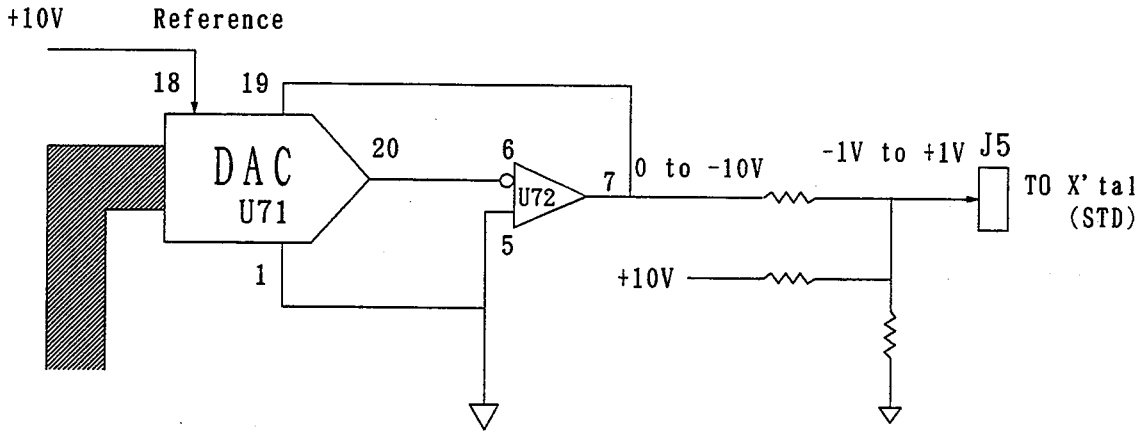


Figure 3.11-8 Frequency Reference Adjustment DAC

The frequency reference adjustment DA converter makes fine adjustments with the standard frequency in the CAL FREQ REF menu available provided by the calibration facility.

Keys adjust the 10MHz reference signal when −1V to +1V are input to the F.ADJ terminal of the STD block (BLK-017041). The variable adjustment range is 3×10^{-7} or more.

3.12 CPU BLOCK

3.12.1 Block Diagram

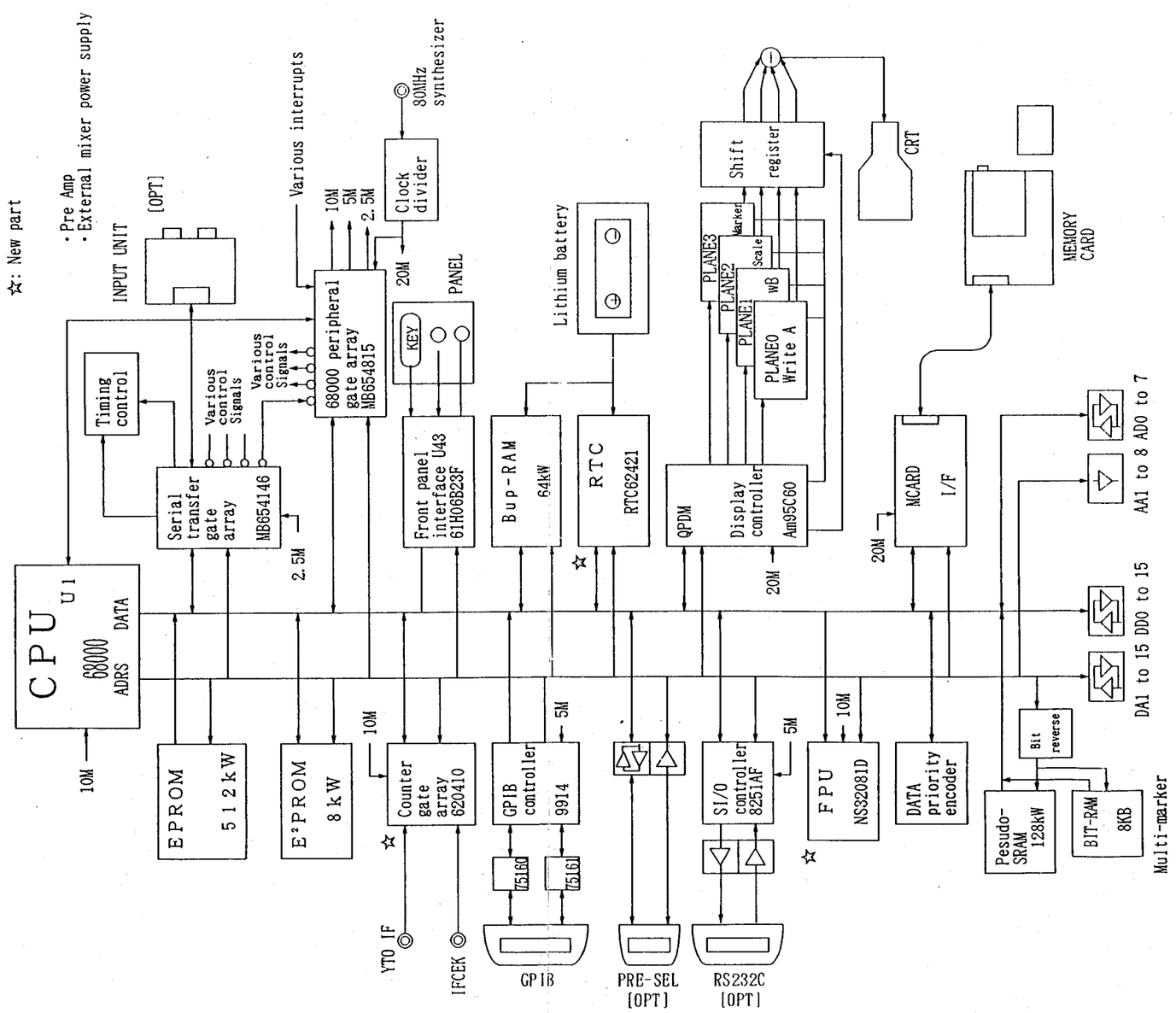


Figure 3.12-1 R3265/3271 CPU Block Diagram

3.12.2 Block Operation Descriptions

CPU (BLS-017500) summaries

① Configuration

The CPU board (BLS-017500) provides basic functions for the R3265/3271. Its components consist of:

ⓐ CPU

ⓑ ROM

ⓒ RAM

ⓓ Display control

ⓔ Key control

ⓕ Clock

ⓖ Counter

Figure 3.12-1 is an overall block diagram of the CPU board.

① Detailed block description

ⓐ CPU

The CPU is a 10MHz version 68000 programmable gate array ceramic package.
A programmed command is generated from address decoders in two gate arrays, and is transmitted to other boards and blocks as a Chip Select signal. The voltage monitoring IC TL7700 is used as for RESET signal generation. When the +5V power supply falls below +4.6V, it issues a * RESET signal to the CPU and other blocks.
DATACK is normally returned to the CPU without a wait time, but only when an analog RF, LOG, IF, or synthesizer command is programmed, * DATACK is returned to the CPU with a 100ns wait time after the command is transmitted.

A block diagram of the CPU peripheral circuitry is shown below.

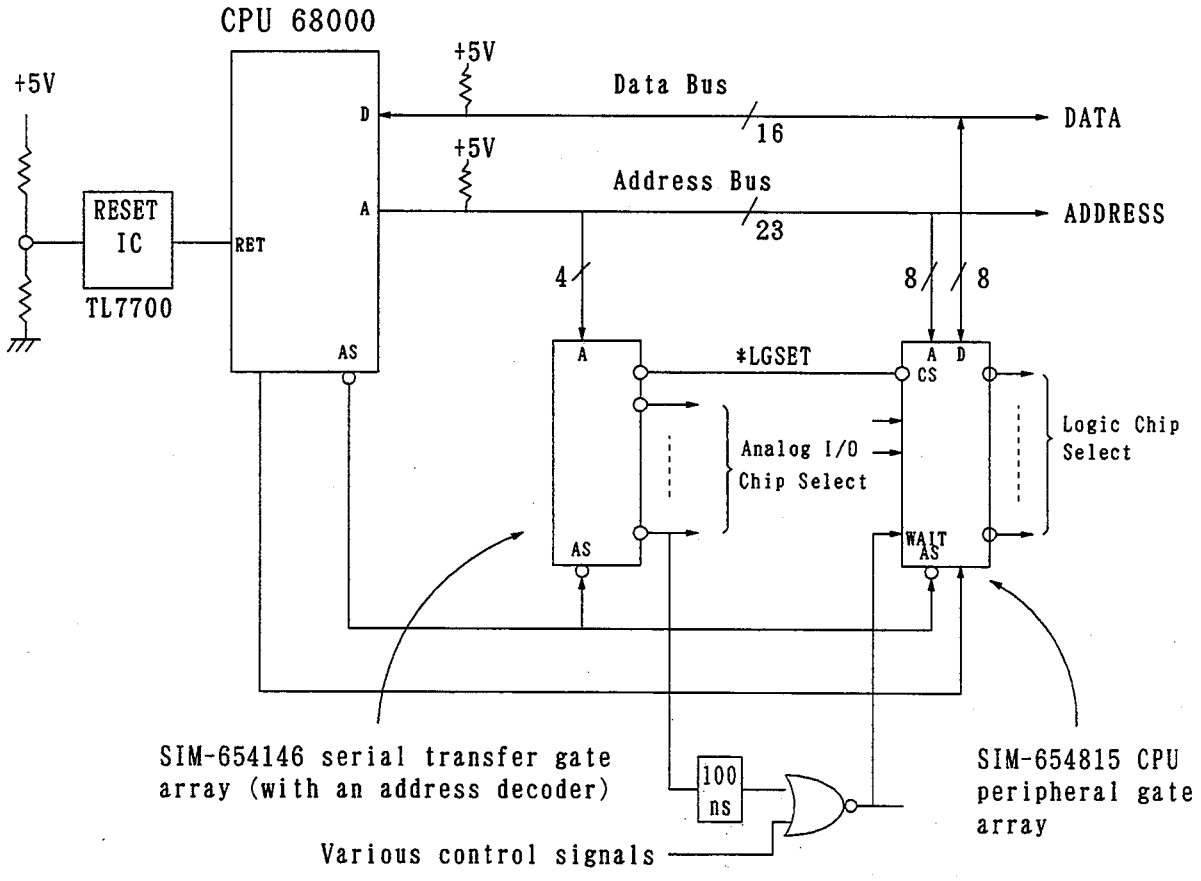


Figure 3.12-2 CPU Peripheral Circuitry Block Diagram

ⓑ ROM

ROM consists of four sets of 2M bit EPROM, SIM-27C2001D15-1. With a 150ns access time, it is organized into 512K by 16 bits.

ⓒ RAM

The CPU board contains four kinds of RAM, as follows:

- Pseudo-RAM, SMM-658128LP12 x 2 (128K words), used as a program, arithmetic, and A/D data storage area. It is designed to share the upper 1K addresses of its storage space with the CPU and A/D board gate array.
- Bit-RAM, SMM-8464CS x 1 (8K bytes), used as marker and sweep stop bit RAM. Since bit-RAM has the upper 1K addresses allocated in the same address space as pseudo-RAM, it can be used to set markers at the addresses corresponding to A/D lamp positions or generate sweep-stop interrupts.
- Battery backup RAM Low-power RAM with battery backup, used to store programmed data or secondary calibration data.

ⓓ Display control

R3265/327 is used as a display controller, and is made of 16 sets of VRAM to hold four screenfuls of data, each consisting of 64k × 16 bits.
Video signal are output as a 0 to 5V analog signal of positive polarity by combining these four screenfuls of data.

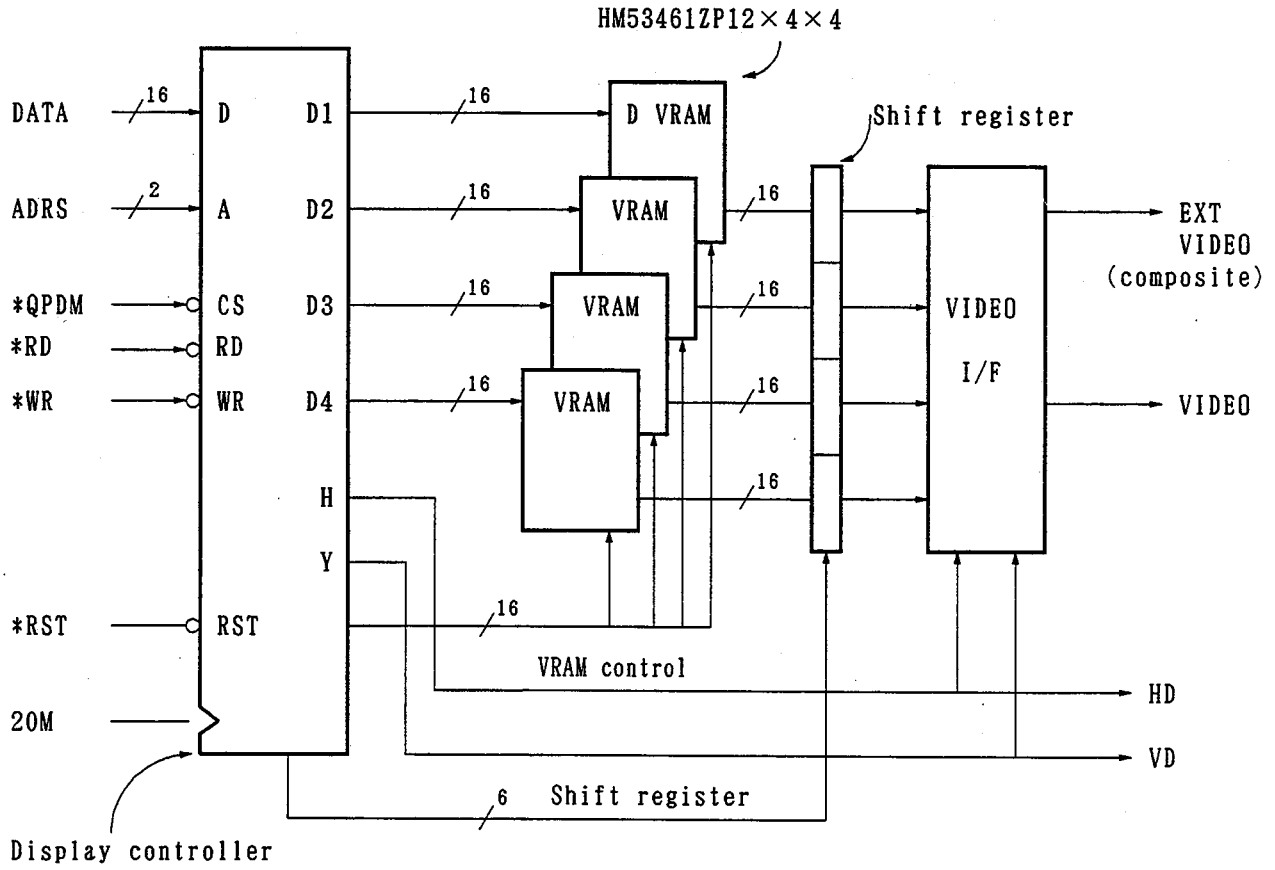


Figure 3.12-3 Display Circuitry

Contents of the four screenfuls of data stored in VRAM
Screen 1: Trace A data
Screen 2: Trace B data
Screen 3: Menu/scale data
Screen 4: Marker data

ⓔ Key control

The key controller gate array controls 43 keys switches, the rotary encoder, and eight LEDs . The key switch codes (in hex) are listed below.

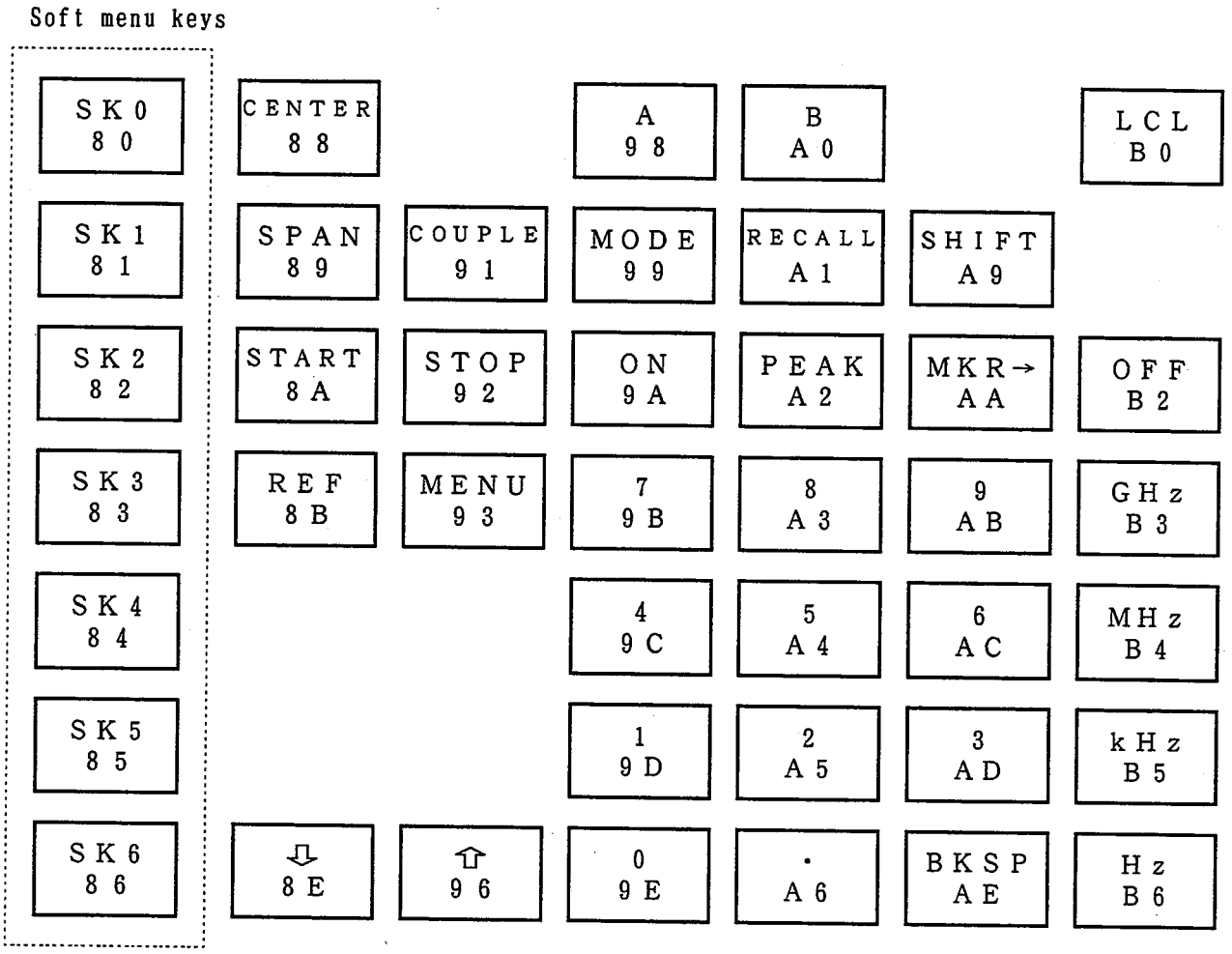


Figure 3.12-4 Key Switch Code

ⓕ Clock

Clock pulses used for the CPU board are generated on the basis of the 80MHz clock produced by dividing the 400MHz reference clock.

The 80MHz clock input, after a TTL level conversion, is divided by four to a 20MHz clock for use as a display and A/D clock. The 20MHz clock is further divided by the CPU peripheral gate array MB654815 to create 10MHz, 5MHz, and 2.5MHz.

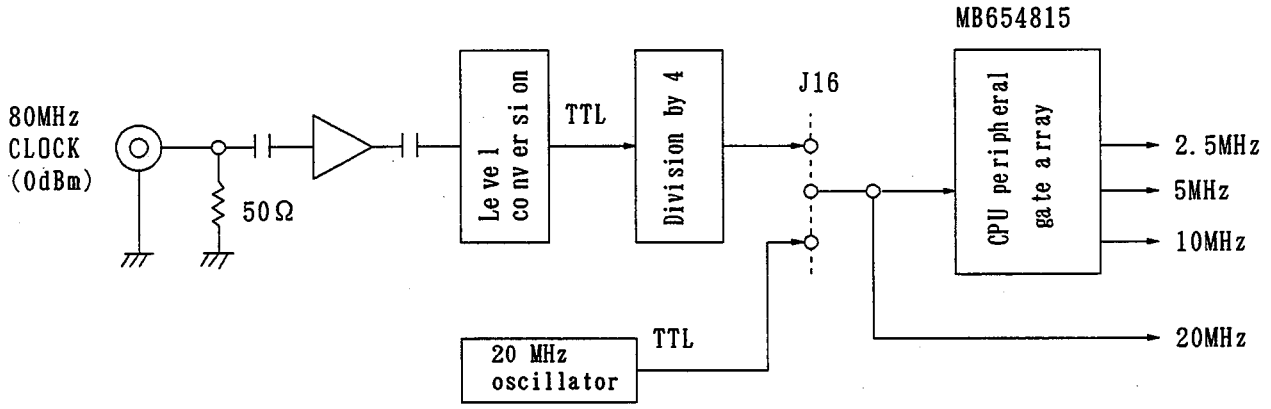


Figure 3.12-5 Clock Block Diagram

20MHz clock:	Display and A/D
10MHz clock:	CPU, FPU, counter (interval timer), and other system timing
5MHz clock:	GPIB and SI/O
2.5MHz clock:	Input unit SI/O

ⓖ Counter

The counter counts the number of IF/YTO IF pulses received during a specified interval timer period.

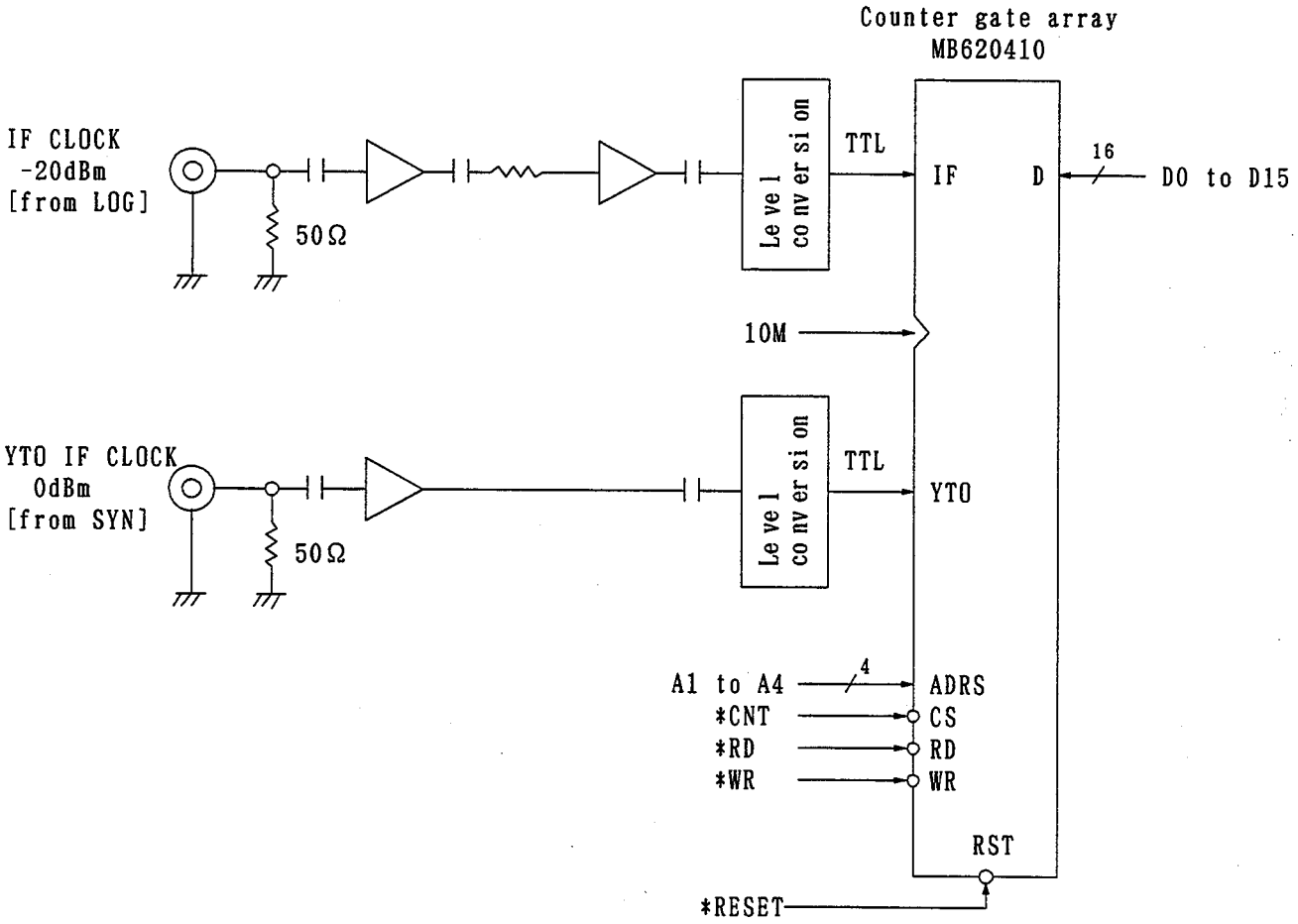


Figure 3.12-6 Counter Block Diagram

MEMO

4. PERFORMANCE TEST (CALIBRATION)

4.1 Introductory Description and UUT Performance Requirements

This procedure describes the performance test of the spectrum analyzer R3265/3271.

The unit being test will be referred to herein as the UUT (Unit-Under-Test).

UUT Environmental range	: TEMP. 20°C to 30°C RH 85% or less
UUT Warm-up/Stabilization period requirements	: 60 minutes

Table 4-1 UUT Performance Requirements (1 of 5)

Unit-Under-Test (UUT) Parameter/Function	Performance Specifications	Test Method
1. Frequency Readout Accuracy and Frequency Countor Marker Accuracy.	Frequency Readout Accuracy: < ± [Counter Frequency × Frequency Reference Accuracy) + (Span × Span Accuracy) + (0.15 × RES.BW) + 10 Hz] Span Accuracy: Span > 2 MHz ± 3% Span ≦ 2 MHz ± 5% Marker Frequency Counter Accuracy: < ± [(Marker Frequency × Frequency Reference Accuracy) + (5 Hz × N) + 1LSD]	Signals are input from the SG where high-precision frequency standard is set as the reference frequency for measurement.
2. Frequency Reference Output Accuracy.	Frequency: $< 1 \times 10^{-7}$/year $< 2 \times 10^{-8}$/day	The frequency of CAL OUT signal locked to the internal 10 MHz reference is measured with the counter.
3. Residual FM	Residual FM: < 3 Hz × Np-p/0.1 sec	Highly stabilized signals are input for measurement.
4. Frequency Drift	Frequency Drift: 2.5 kHz × Sweep Time (min.) × N (50 kHz < Span ≦ 2 MHz) 60 Hz × Sweep Time (min.) × N (Span ≦ 50 kHz)	Highly stabilized signals are input for measurement.
5. Noise Sidebands	f ≦ 2.6 GHz: 1 kHz offset < −100 dBc/Hz 10 kHz offset < −110 dBc/Hz 20 kHz offset < −110 dBc/Hz 100 kHz offset < −114 dBc/Hz f > 2.6 GHz: 1 kHz offset < (−95 + 20 logN) dBc/Hz 10 kHz offset < (−108 + 20 logN) dBc/Hz 20 kHz offset < (−108 + 20 logN) dBc/Hz 100 kHz offset < (−110 + 20 logN) dBc/Hz	Good noise sideband signals are input for measurement.
6. Frequency Span Accuracy	Linear Span: < ± 3% (Span > 2 MHz) < ± 5% (Span ≦ 2 MHz) Log Span: ± (10 + Stop Frequency × 0.1%)	Signals at two frequencies according to each span are input to measure the difference between the frequencies.

Table 4-1 UUT Performance Requirements (2 of 5)

Unit-Under-Test (UUT) Parameter/Function	Performance Specifications	Test Method
7. Resolution Bandwidth Accuracy and Selectivity	Range Accuracy: 10 Hz to 3 MHz 1, 3, 10 sequence ±15% 100 Hz to 1 MHz ±25% 30 Hz (25°C ± 10°C), 3 MHz ±50% 10 Hz to 100 Hz nominal (digital IF) Selectivity (−60 dB/−3 dB): <15:1 100 Hz to 3 MHz <20:1 30 Hz 5:1 10 Hz to 100 Hz nominal (digital IF) Bandwidth (−6 dB): 200 Hz, 9 kHz, 120 kHz Conformed to CISPR standard	CAL OUT signals are input for measurement.
8. Resolution Bandwidth Switching Uncertainty	100 Hz to 3 MHz RBW: < ±0.3 dB (Reference to 300 kHz RBW) 30 Hz RBW : < ±1 dB (digital IF) 10 Hz to 100 Hz : < ±1.5 dB	CAL OUT signals are input for measurement.
9. Displayed Average Noise Level	(10 Hz res BW, 0 dB input atten, 1 Hz video filter) R3265: −100 dBm 1 kHz −110 dBm 10 kHz −111 dBm 100 kHz −135 dBm 1 MHz −{140 − 1.55f(GHz)} dBm 10 MHz to 3.6 GHz −{145 − 1.55f(GHz)} dBm 10 MHz to 3.6 GHz (Low noise mode) −135 dBm 3.5 GHz to 8 GHz R3271: −100 dBm 1 kHz −110 dBm 10 kHz −111 dBm 100 kHz −{135 − 1.55f(GHz)} dBm 1 MHz to 3.6 GHz −130 dBm 3.5 GHz to 7.5 GHz −123 dBm 7.4 GHz to 15.4 GHz −116 dBm 15.2 GHz to 23.3 GHz −110 dBm 23 GHz to 26.5 GHz	No signal is input and average noise level at each frequency is measured.

Table 4-1 UUT Performance Requirements (3 of 5)

<table>
<tr><th>Unit-Under-Test (UUT) Parameter/Function</th><th>Performance Specifications</th><th>Test Method</th></tr>
<tr><td>10. Gain Compression (1 dB)</td><td>R3265:
−5 dBm mixer input level > 200 MHz
−10 dBm mixer input level > 10 MHz

R3271:
−5 dBm mixer input level > 10 MHz</td><td>Two signals are input simultaneously to measure the level at which one of the signals is lowered by 1 dB.</td></tr>
<tr><td>11. Residual Response</td><td>(no signal at input, 0 dB RF Attenuation)
R3265:
<table><tr><td>< −100 dBm</td><td>1 MHz</td></tr><tr><td>< −90 dBm</td><td>300 kHz</td></tr></table>
R3271:
<table><tr><td>< −100 dBm</td><td>1 MHz to 3.6 GHz</td></tr><tr><td>< −90 dBm</td><td>300 kHz to 26.5 GHz</td></tr></table></td><td>No signal is input and the test is terminated at 50 Ω.</td></tr>
<tr><td>12. Second Harmonic Distortion</td><td>R3265:
<table><tr><th></th><th>freq range</th><th>mixer level</th></tr><tr><td>< −70 dBc</td><td>100 MHz to 3.6 GHz</td><td>−30 dBm</td></tr><tr><td>< −60 dBc</td><td>10 MHz to 3.6 GHz</td><td>−30 dBm</td></tr><tr><td>< −100 dBc</td><td>>3.5 GHz</td><td>−10 dBm</td></tr></table>R3271:
<table><tr><th></th><th>freq range</th><th>mixer level</th></tr><tr><td>< −70 dBc</td><td>10 MHz to 3.6 GHz</td><td>−30 dBm</td></tr><tr><td>< −100 dBc</td><td>>3.5 GHz</td><td>−10 dBm</td></tr></table></td><td>The lowpass filter is connected to the SG output for measurement.</td></tr>
</table>

Table 4-1 UUT Performance Requirements (4 of 5)

<table>
<tr><th>Unit-Under-Test (UUT) Parameter/Function</th><th>Performance Specifications</th><th>Test Method</th></tr>
<tr><td>13. Third Order Intermodulation Distortion</td><td>R3265:
<table><tr><th></th><th>freq range</th><th>mixer level</th></tr><tr><td>< −70 dBc</td><td>200 MHz to 3.6 GHz</td><td>−30 dBm</td></tr><tr><td>< −60 dBc</td><td>10 MHz to 3.6 GHz</td><td>−30 dBm</td></tr><tr><td>< −75 dBc</td><td>>3.5 GHz</td><td>−30 dBm</td></tr></table>R3271:
<table><tr><th></th><th>freq range</th><th>mixer level</th></tr><tr><td>< −70 dBc</td><td>10 MHz to 3.6 GHz</td><td>−30 dBm</td></tr><tr><td>< −75 dBc</td><td>>3.6 GHz</td><td>−30 dBm</td></tr></table></td><td>Two neighboring signals are input simultaneously for measurement.</td></tr>
<tr><td>14. Image, Multiple, Out of Band Response</td><td>R3265:
< −70 dBc (10 MHz to 8 GHz)

R3271:
< −70 dBc (10 MHz to 18 GHz)
< −60 dBc (10 MHz to 23 GHz)
< −50 dBc (10 MHz to 26.5 GHz)</td><td>Signals allowing image, multiple and out of band response as against the center frequency are input for measurement.</td></tr>
<tr><td>15. Frequency Response</td><td>10 dB input attenuation
R3265:
±1.5 dB 100 Hz to 3.6 GHz
±1.0 dB 50 MHz to 2.6 GHz
±1.5 dB 3.5 GHz to 7.5 GHz
±1.5 dB 7.4 GHz to 8 GHz
Additional Uncertainly Due to Band Switching:
±0.5 dB
Frequency Response Referenced to CAL Signal:
±5 dB 100 Hz to 8 GHz
R3271:
±1.5 dB 100 Hz to 3.6 GHz
±1.0 dB 50 MHz to 2.6 GHz
±1.5 dB 3.5 GHz to 7.5 GHz
±3.5 dB 7.4 GHz to 15.4 GHz
±4.0 dB 15.4 GHz to 23.3 GHz
±4.0 dB 23 GHz to 26.5 GHz
Additional Uncertainly Due to Band Switching:
±0.5 dB
Frequency Response Referenced to CAL Signal:
±5 dB 100 Hz to 26.5 GHz</td><td>The signal level of SG at a certain level on the screen is measured at each frequency with the power meter.</td></tr>
</table>

Table 4-1 UUT Performance Requirements (5 of 5)

Unit-Under-Test (UUT) Parameter/Function	Performance Specifications	Test Method
16. IF Gain Uncertainty	(after automatic calibration) ±0.5 dB 0 dBm to −50 dBm ±0.7 dB 0 dBm to −80 dBm	The REF level is raised while lowering the signal level with the external attenuator to measure the error.
17. Scale Fidelity	Log: ±0.2 dB/1 dB, ±1 dB/10 dB, ±1.5 dB/90 dB Linear: ±5% of reference level QP Mode Log: ±1.0 dB/30 dB, ±2 dB/40 dB, ± 1.0 dB/40 dB (25°C ± 10°C)	Input signal is lowered with the external attenuator for measurement.
18. Input Attenuator Accuracy	(20 dB to 70 dB settings referenced to 10 dB) R3265: ±1.1 dB/10 dB step, 2.0 dB max, 100 Hz to 8 GHz R3271: ±1.1 dB/10 dB step, 2.0 dB max, 100 Hz to 12.4 GHz ±1.3 dB/10 dB step, 2.5 dB max, 12.4 GHz to 18 GHz ±1.8 dB/10 dB step, 3.5 dB max 18 GHz to 26.5 GHz	Signal at a frequency is input and measured with the internal attenuator.
19. Sweep Time Accuracy	Accuracy: < ±3%	Square wave signals at a known frequency are input repeatedly according to each sweep time for sweep time measurement.
20. Calibration Amplitude Accuracy	Amplitude: −10 dBm ± 0.3 dB	CAL OUT signals are measured with the power meter.

4.2 Measurement Standards and Support Test Equipment Performance Requirement

Minimum-Use-Specifications (MUS) are the calculated minimum performance specifications criteria needed for the Measurement Standards (MS) and support M&TE to be used for the comparison measurements required in the Test Procedure (TP) process.

The MUS is developed through uncertainty analysis and is calculated through assignment of a defines and documented uncertainty/accuracy ratio or margin between the specified tolerances of the UUT and the capability (uncertainty specification) required of the measurement standards system. MUS is required to assist a measurement specialist in the evaluation of existing or selection of alternate measurement standards equipment.

The uncertainty/accuracy ratio applied in this TP is 10:1 and any exception to that is indicated in Section 4.1.

CAUTION

The instructions in this TP relate specifically to the equipment and conditions listed in Section 4.2. If other equipment is substituted, the information and instructions must be interpreted and revised accordingly.

MS and SM&TE Environmental Range	:	Temperature	:	18°C to 28°C
	:	Relative Humidity	:	30% to 70%
MS and SM&TE Warm-up/Stabilization Period Requirements			:	60 minutes

Table 4-2 Measurement Standards (MS) Performance Requirements

Equipment Generic Name (Qty)	Minimum-Use-Specifications	Mfr., Model/Option Applicable
Frequency Standard	Output Frequency : 10 MHz Stability : 5×10^{-10}/day Output Impedance : about 50 Ω Output Voltage : 1 Vpp or more	TR3110
Synthesized Sweeper	Frequency Range : 10 MHz to 18 GHz Frequency Accuracy (CW): 3×10^{-8}/day Power Level Range : −15 dBm to +15 dBm	TR4515
Frequency Counter	Frequency Range : 10 Hz to 120 MHz Gate Time : 10s Number of Digits Displayed : 8 digits Input Voltage Range : 25 mVrms to 500 mVrms	TR5823
Frequency Synthesizer	Frequency Range : 10 MHz to 20 MHz Stability : 5×10^{-6}/year Power Level Range : −10 dBm to +13 dBm	HP3325
Synthesized Signal Generator	Frequency Range : 10 MHz to 4 GHz Residual SSB Phase Noise: 1 kHz offset < −115 dBc/Hz 10 kHz offset < −125 dBc/Hz 100 kHz offset < −130 dBc/Hz Power Level Range : −20 dBm to +10 dBm	R4262
Power Meter	Accuracy : ±0.02 dB (dB Relative Mode)	HP436A
Power Sensor	Frequency Range : 50 MHz to 26.5 GHz Power Range : 1 µW to 100 mW Maximum SWR : 1.25 (26.5 GHz)	HP 8485A
	Frequency Range : 10 MHz to 18 GHz Power Range : 1 µW to 10 mW	HP8481A
Sweeper	Frequency Range : 10MHz to 26.5 GHz Power Range : −5 dBm to +10 dBm (at 3.6 GHz)	HP8350 + HP83595A
1 dB Step Attenuator	Frequency Range : DC to 18 GHz Attenuation Range : 12 dB	HP8494H
10 dB Step Attenuator	Frequency Range : DC to 18 GHz Attenuation Range : 70 dB	HP8495H
Attenuator Driver		HP11713A

Table 4-3 Support Measuring & Test Equipment (M&TE) Performance Requirements

Equipment Generic Name (Qty)	Minimum-Use-Specifications	Mfr., Model/Option Applicable
Adapter	Type N(m) to BNC(f)	Generic
	Type N(m) to SMA(f)	Generic
	SMA(m) to SMA(m)	50-673-0000-31 (Sealectro)
	Type N(f) to BNC(m)	Generic
50 Ω Termination	SMA	Generic
20dB Fixed, 3dB Fixed Attenuator	Connector : SMA(m), SMA(f)	Generic
Power Splitter	Frequency Range : 10 MHz to 26.5 GHz Insertion Loss : 6 dB (nominal)	Model 1579 (Weinschel)
Low-pass Filter	Cutoff Frequency : 2.2 GHz Rejection at 3 GHz : >40 dB Rejection at 3.8 GHz: >80 dB	
Power Divider	Frequency Range : 10 MHz to 300 MHz Isolation : >20 dB	H-8-4 (ANZAC)
	Frequency Range : 2 GHz to 4 GHz Isolation : >20 dB	4313-2 (NARDA)
Cable	Frequency Range : DC to 26.5 GHz Maximum SWR : <1.45 GHz at 26.5 GHz Length : about 70 cm Connector : SMA(m) both ends	A01002
	Length : 150 cm Connector : BNC(m) both ends	MI-09
	Length : 10 cm Connector : BNC(m) both ends	MC-61

4.3 Preliminary Operations

WARNING

Always makes sure spectrum analyzer's power supply cord is plugged into a 3-hole grounded outlet or 2-hole outlet with grounded adapter. You can be fatally shocked if you fail to follow this rule.

Do not touch live circuits when calibrating instrument.

(1) Review this entire procedure before starting calibration procedure.

(2) Always confirm that the POWER switch is OFF before connecting the power cable to the AC line.

4.4 Performance Test Process

4.4.1 Accuracy of Frequency Readout and Frequency Counter Marker

- SPECIFICATION

  Frequency Readout Accuracy < ± [(Center Frequency × Frequency Reference Accuracy) + (Span × Span Accuracy) + (0.15 × RES.BW) + 10 Hz]

  Span Accuracy: Span > 2MHz ±3%
  Span ≤ 2MHz ±5%

  Marker Frequency Counter Accuracy < ± [(Marker Freq. × Freq. Reference Accuracy) + (5 Hz × N) + 1 LSD]

- RELATED ADJUSTMENT
  YTO Adjustment
  10 MHz Frequency Reference Adjustment

- DESCRIPTION
  The accuracy of the R3265/3271 frequency readout and frequency counter marker is tested with an input signal of known frequency.

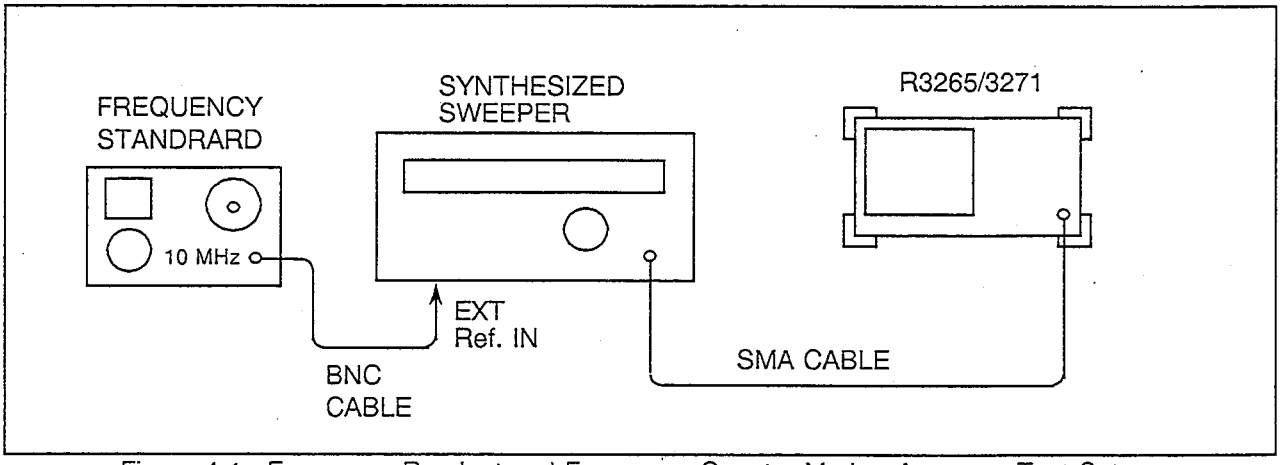


Figure 4-1 Frequency Readout and Frequency Counter Marker Accuracy Test Setup

- EQUIPMENT

  Frequency Standard TR3110
  Synthesized Sweeper TR4515

  Cables:
  SMA, 70 cm A01002
  BNC, 150 cm MI-09

- PROCEDURE

(1) Connect the equipment as shown in Figure 4-1

[Frequency Readout Accuracy]

(2) Press the INSTRUMENT [PRESET] key on the TR4515. Set the TR4515 controls as follows:

CW	2 GMz
Power Level	−10 dBm
Frequenty Reference	EXT (Rear Panel)

(3) On the R3265/3271, press the [PRESET] key and set the controls as follows:

Center Freq	2 GHz
Span	1 MHz

(4) On the R3265/3271, press the [PEAK] key. Record the MKR frequency on Table 4-4 as the Actual Marker Reading. The reading should be within the limits shown.

(5) Repeat step (4) for all the frequency and span combinations listed in Table 4-4. Peak the R3265/3271 preselector for and set the Analyzer and the TR4515's [CW] key to frequencies of 5 GHz and above.

[Frequency Counter Marker Accuracy]

(6) Set the [FREQ SPAN] key of the R3265/3271 to 1 MHz.

Press the MARKER [ON] key to [COUNTER] and [CNT RES 1 Hz].

(7) Key in the TR4515 [CW] frequencies and the R3265/R3271 center as indicated in Table 4-5. For each pair of settings, press the [PEAK] key and record the MKR frequency at each point in Table 4-5.
The marker readings should be within the limits shown.

Table 4-4 Frequency Readout Accuracy

TR4515 Frequency (GHz)	R3265/3271		Marker Reading		
	Span	Center Frequency	Min. (GHz)	Actual (GHz)	Max. (GHz)
2	1 MHz	2 GHz	1.999948		2.000051
2	10 MHz	2 GHz	1.99968		2.00031
2	20 MHz	2 GHz	1.99935		2.00064
2	50 MHz	2 GHz	1.99845		2.00154
2	100 MHz	2 GHz	1.9968		2.0031
2	2 GHz	2 GHz	1.939		2.060
5	1 MHz	5 GHz	4.999947		5.000052
5	10 MHz	5 GHz	4.99968		5.00031
5	20 MHz	5 GHz	4.99935		5.00064
5	50 MHz	5 GHz	4.99845		5.00154
5	100 MHz	5 GHz	4.9968		5.0031
5	2 GHz	5 GHz	4.939		5.060
<R3271 ONLY>					
11	1 MHz	11 GHz	10.999947		11.000052
11	10 MHz	11 GHz	10.99968		11.00031
11	20 MHz	11 GHz	10.99935		11.00064
11	50 MHz	11 GHz	10.99845		11.00154
11	100 MHz	11 GHz	10.9968		11.0031
11	2 GHz	11 GHz	10.939		11.060
18	1 MHz	18 GHz	17.999946		18.000053
18	10 MHz	18 GHz	17.99968		18.00031
18	20 MHz	18 GHz	17.99935		18.00064
18	50 MHz	18 GHz	17.99845		18.00154
18	100 MHz	18 GHz	17.9968		18.0031
18	2 GHz	18 GHz	17.939		18.060

Table 4-5 Frequency Counter Marker Accuracy

TR4515 Frequency (GHz)	R3265/3271 Center Frequency (GHz)	Marker Frequency		
		Min.(GHz)	Actual(GHz)	Max.(GHz)
2	2	1.999999794		2.000000206
5	5	4.999999494		5.000000506
<R3271 ONLY>				
11	11	10.999998889		11.000001111
18	18	17.999998184		18.000001816

4.4.2 Frequency Reference Output Accuracy

- SPECIFICATION

  Frequency: $<1\times10^{-7}$/year, $<2\times10^{-8}$/day

- RELATED ADJUSTMENT

  Frequency Reference Adjustment

- DESCRIPTION

  The 10 MHz reference signal is measured for frequency accuracy by measuring the frequency of the 25 MHz CAL OUTPUT signal. The CAL OUTPUT signal is referenced to the10 MHz reference.

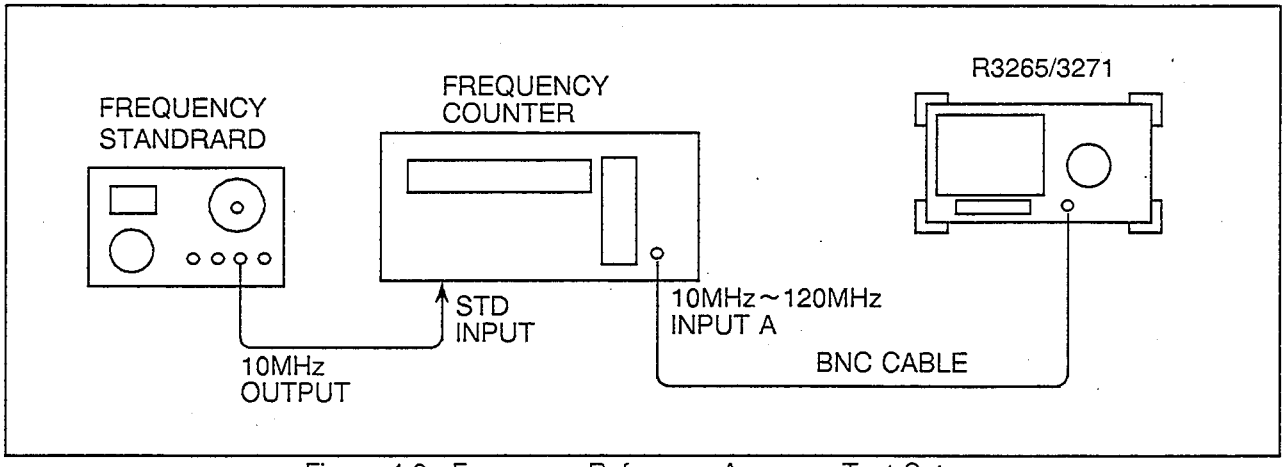


Figure 4-2 Frequency Reference Accuracy Test Setup

- EQUIPMENT

  Frequency Counter TR5823
  Frequency Standard TR3110

  Cables:

  BNC, 150 cm (2 required) MI-09

- PROCEDURE

(1) Connect the equipment as shown in Figure 4-2.

(2) Set the TR5823 controls as follows:

FREQUENCY STD SWITCH (Rear Panel)	EXT
INPUT CHANNEL	INPUT A
GATE TIME	10 sec

(3) Press the PRESET key on the R3265/3271.

CAUTION

Before starting this measurement, perform warm-up operation of the R3265/3271 for more than 30 minutes. If the frequency reference of the R3265/3271 is set to EXT, set it to INT or perform 15-minute warm-up operation after instrument preset.

(4) Wait for the frequency counter to settle down.

(5) Read the frequency counter display. The frequency should be within the following limits:

(2)*4.9999975 ≤ _____ ≤ (2)*5.0000025

*: The counter can display only eight digits.

4.4.3 Residual FM

- SPECIFICATION

  Residual FM: < 3 Hz × Np-p/0.1 sec

- RELATED ADJUSTMENT

  There is no related adjustment procedure for this performance test.

- DESCRIPTION

  The Residual FM Test measures the short-term stability of the spectrum analyzer's LO system. A stable signal is applied to the input. In zero span, the signal is slope detected on the IF bandwidth filter skirt. Any instability in the LO system transfers to the IF signal in the mixing process. The test determines the slope of the IF filter in Hz/dB and then measures the signal amplitude variation caused by the residual FM. Multiplying these two values gives the residual FM in Hz.

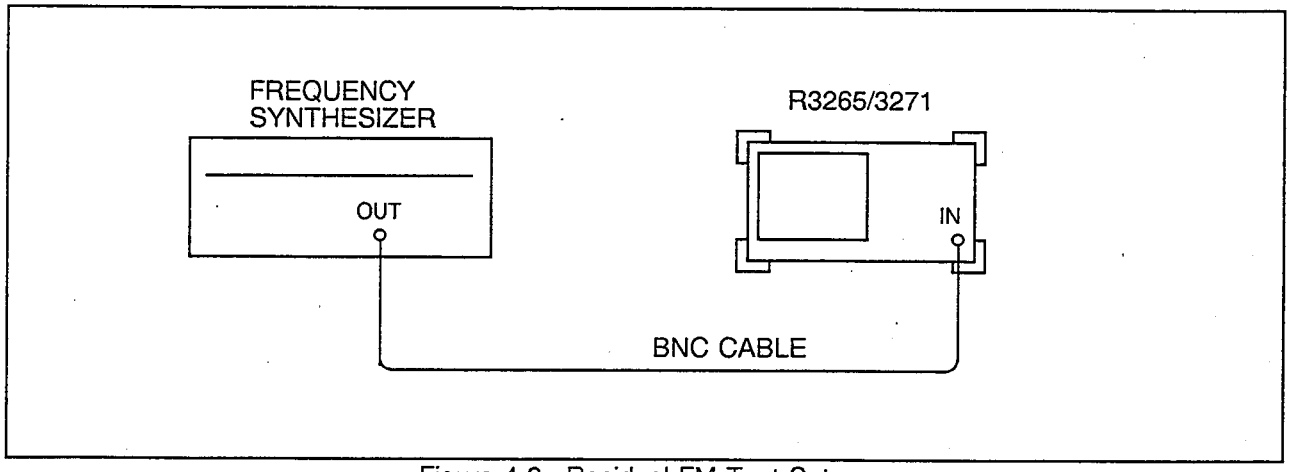


Figure 4-3 Residual FM Test Setup

- EQUIPMENT

  Frequency Synthesizer HP3325

  Cable:

  BNC, 150 cm MI-09

- PROCEDURE

[Determining the IF Filter Slope]

(1) Connect the equipment as shown in Figure 4-3.

(2) Set the Frequency Synthesizer controls as follows:

FREQ	10 MHz
AMPTD	−10 dBn
FUNCTION	~ key

(3) On the R3265/3271, press the [PRESET] key and set the [CENTER FREQ] to 10 MHz, [FREQ SPAN] to 100kHz.
Press the [CPL] key and [NEXT MENU], then press [DIGITAL IF 1/2/OFF] twice to set the Digital IF to "OFF".
Press the [PEAK] key, marker [ON] key, [SIG TRK ON/OFF] to set the signal track to "ON".

Press the [FREQ SPAN] key, then press [↓] six times to set the SPAN to 1kHz.

Set the [RBW] to 30 Hz.

Press the MARKER [ON] key, [SIG TRK ON/OFF] to set the signal track to "OFF".

Set the [REF LEVEL] −5 dBm and [dB/div] to 1 dB, and set [FREQ SPAN] to 200 Hz.

Press the [PEAK] key, [MKR→] key, [MKR→REF] and [PEAK] [MKR→] [MKR→REF].

Press the [MENU] key, [SWEEP MODE] and [SINGLE SWP].

Press [ON] [⊿MKR].

(4) Rotate the data entry knob clockwise until MKR reads −3 dB ± 0.1 dB.
Press [⊿MKR]. Rotate the data entry knob clockwise until MKR read −6 dB ± 0.1 dB.

(5) Divide the ⊿MKR frequency by the ⊿MKR amplitude to obtain the slope of the RBW filter. For example, if the ⊿MKR frequency is 14 Hz and the ⊿MKR amplitude is 6.05 dB, the slope is 2.3 Hz/dB.
Record the result below:

Slope_____Hz/dB

[Measuring the Residual FM]

(6) Press the MARKER [OFF] key, the [MENU] key, [SWEEP MODE] and [CONT SWP].
Set [FREQ SPAN] to 0 Hz.

Set the SWEEP to 100 ms.

(7) Press the [CENTER FREQ] key. Rotate the data entry knob clockwise to place the displayed trace about six divisions below the reference level.

Press the [MENU] key, [SWEEP MODE] and [SINGLE SWP].

Press the [PEAK] key, MARKER [ON] key [⊿ MKR] and [PEAK] key [MIN].

(8) Read the ⊿ MKR amplitude, take its absolute value, and record the result as the deviation.

Deviation: _____dB

(9) Calculate the residual FM by multiplying the slope recorded before by the deviation. Record the result below.
The residual FM should be less the 3 Hz.

Residual FM: _____Hz

4.4.4 Frequency Drift

- SPECIFICATION

Frequency Drift —
- 2.5 kHz × sweep time (min) × N (50 kHz < span ≤ 2 MHz)
- 60 Hz × sweep time (min) × N (span ≤ 50 kHz)

- RELATED ADJUSTMENT

  There is no related adjustment procedure for this performance test.

- DESCRIPTION

  In the frequency drift test, drift of the spectrum analyzer's LO system is measured when the sweep time is long. Drifts are measured for two spans by inputting highly-stabilized signal.

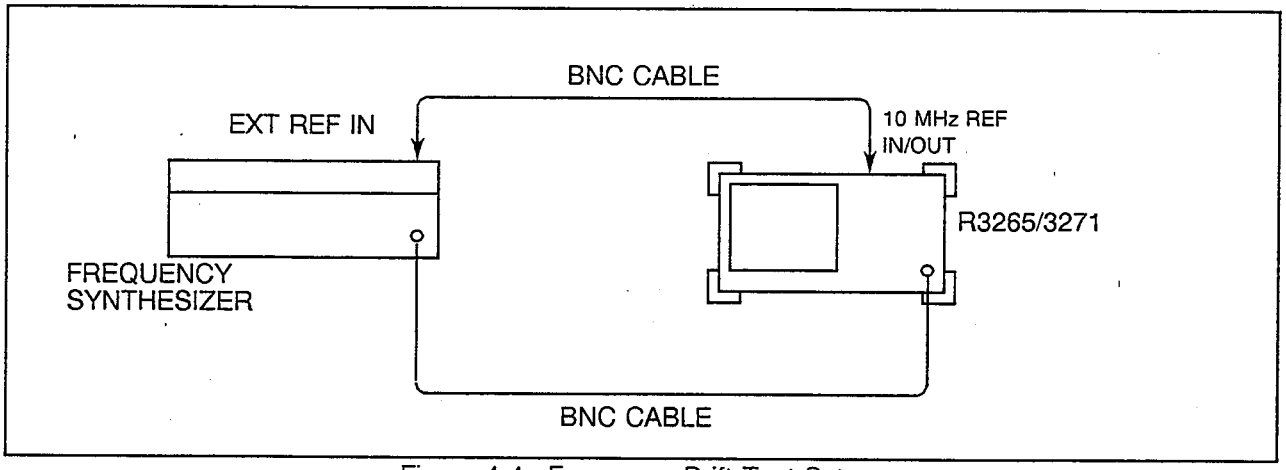


Figure 4-4 Frequency Drift Test Setup

- EQUIPMENT

Frequency Synthesizer HP3325

Cable: BNC 150 cm (2 required) MI-09
Adapter: Type (N) to BNC

- PROCEDURE

(1) Connect the equipment as shown in Figure 4-4.

(2) On the HP3325, set the controls as follows:

FREQ	10 MHz
AMPTD	−8 dBm
FUNCTION	~ key

(3) On the R3265/3271, press [PRESET] and set the controls as follows:

CENTER FREQ	10 MHz
SPAN	50.1 kHz
dB/div	2 dB/div
SWP	1 sec

(4) On the R3265/3271, press [CENTER FREQ], [↓], [↓], [↓] and the signal on the screen moves to the second division from the right. Wait for sweep to be performed three times or more.

(5) On the R3265/3271, press [A] [VIEW A] and [B] [WRITE B].
Set the sweep time to 80 sec.

Press [MENU] [SWEEP MODE] [SINGLE SWP] [RESET SWP].
Wait for the sweep to be completed (until the sweep indicator goes off).

(6) On the R3265/3271, press [PEAK], MARKER, [ON], [Δ MKR], [A] and [PEAK].

(7) Read the MKR frequency and record this as the frequency drift.
It should be less than 2.5 kHz.

Frequency Drift: _____Hz

(8) On the R3265/3271, press [MENU], [SWEEP MODE], [CONT SWP] and MARKER [OFF].

Press [A] [WRITE A], [B] [BLANK B] and [CPL], [SWP], [AUTO], [NEXT MENU], [DIGITAL IF 1/2/OFF], [DIGITAL IF 1/2/OFF] to set to the DIGITAL IF to "OFF".

Set the R3265/3271 as follows:

Center Freq	10 MHz
Span	200 Hz
RBW	30 Hz
SWP	5 sec

Wait for sweep to be performed three times or more.

(9) Repeat (4) through (6).

(10) Read the MKR frequency and record this as the frequency drift.
It should be less than 60 Hz.

Frequency Drift: _____Hz

4.4.5 Noise Sidebands

- SPECIFICATION

  Noise Sidebands:

Offset	f ≤2.6 GHz	f>2.6 GHz
1 kHz	< −100 dBc/Hz	< (−95 + 20 logN) dBc/Hz
10 kHz	< −110 dBc/Hz	< (−108 + 20 logN) dBc/Hz
100 kHz	< −114 dBc/Hz	< (−110 + 20 logN) dBc/Hz

- RELATED ADJUSTMENT

  There is no related adjustment procedure for this performance test.

- DESCRIPTION

  The noise sidebands of a 2.6 GHz and 3.7 GHz, −10 dBm, signal are measured at an offset of 1 kHz, 10 kHz and 100 kHz from the carrier.

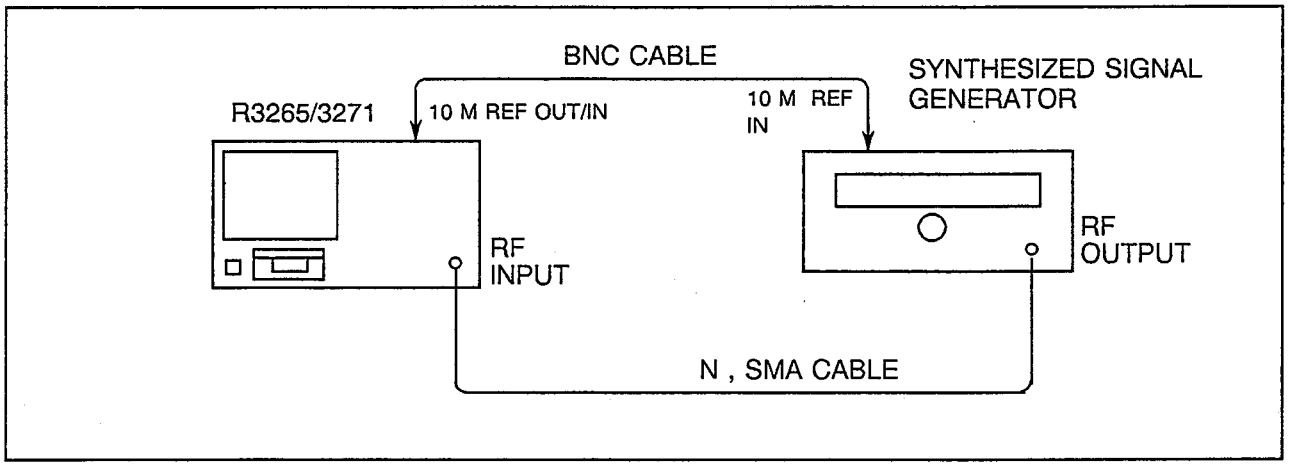


Figure 4-5 Noise Sidebands Test Setup

- EQUIPMENT: Synthesized Signal Generator

Critical Specifications for Equipment Substitution	Recommended model
Frequency Range = 10 MHz to 4 GHz Residual SSB Phase Noise at 1 kHz offset < −115 dBc/Hz 10 kHz offset < −125 dBc/Hz 100 kHz offset < −130 dBc/Hz	R4262

- PROCEDURE

(1) Connect the equipment as shown in Figure 4-5.

(2) Set the Signal Generator controls as follows:

Frequency ..... 2.6 GHz & 3.7 GHz
CW Output ..... −5 dBm

(3) Press the [PRESET] key on the R3265/3271. Press the [CPL] key and [NEXT MENU], then press [DIGITAL 1/2/OFF] twice, to set the Digital IF to "OFF".

Set [CENTER FREQ] to 2.6GHz.

Since the measurement is made for each of 1 kHz, 10 kHz and 100 kHz offset frequency, set the span frequency to 2.5 times each offset frequency, or 2.5 kHz, 25 kHz and 250 kHz. Keep other settings unchanged.

(4) Operate keys on the R3265/3271 as follows to measure noise sidebands of each offset frequency. The measurement procedure for 100 kHz offset frequency is explained here, and the procedure is applicable for 10 kHz and 1 kHz offset frequency.

Set the span corresponding to offset.

Press the [PEAK] key and the [MKR→] key [MKR→ REF].

Press the [PEAK] key and the MARKER [ON] key [NOISE/ XHz] and [dBc/Hz].

Press [1] [0] [0] [kHz] to set each offset frequency.

Press the reference level by 20 dB and perform averaging for about 20 samples. After averaging, read the marker level and write it down in Table 4-6.

Also, measure noise sidebands with the center frequency at 3.7 GHz, and Table 4-6 is completed.

Table 4-6 Noise Sidebands

Offset (kHz)	CF 2.6 GHz		CF 3.7 GHz	
	Actual (dBc/Hz)	Max. (dBc/Hz)	Actual (dBc/Hz)	Max. (dBc/Hz)
1		−100		−95
10		−110		−108
100		−114		−110

4.4.6 Frequency Span Accuracy

- SPECIFICATION
  - < ± 3% of actual frequency separation (SPAN > 2 MHz)
  - < ± 5% of actual frequency separation (SPAN ≤ 2 MHz)
  - < ± (10% of actual frequency + 0.1% of Stop frequency): LOG Span Accuracy

- RELATED ADJUSTMENT
  Span adjustment.

- DESCRIPTION

  Set the signal frequency twice with the synthesized sweeper and measure the difference between signal frequencies with the analyzer.
  Check the span accuracy using the signal frequency difference measured with the ⊿MARKER function.

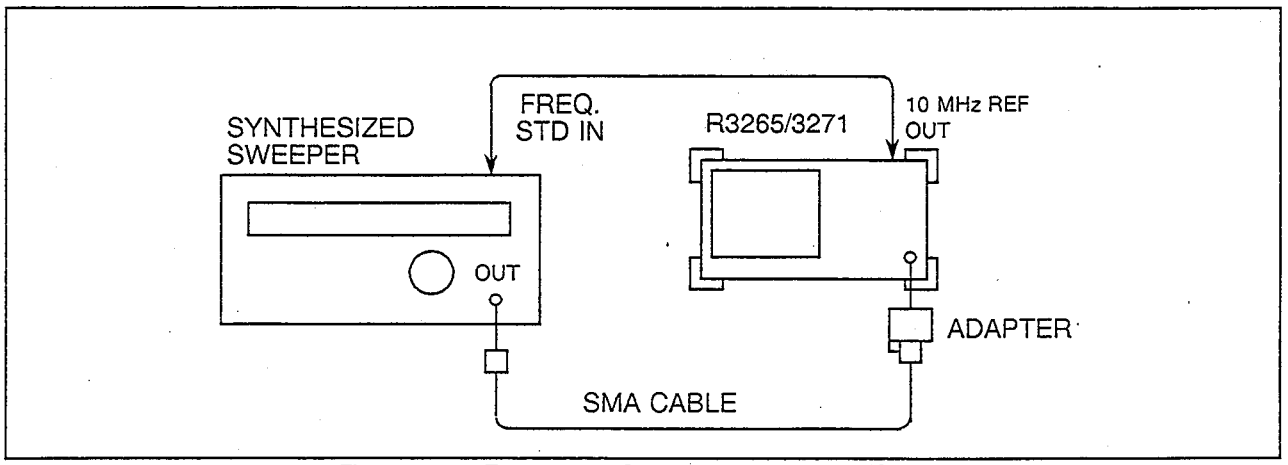


Figure 4-6 Frequency Span Accuracy Test Setup

- EQUIPMENT

Synthesized Sweeper	TR4515
Cables:	
SMA, 70 cm	A01002
BNC, 150 cm	MI-09

- PROCEDURE

(1) Connect the equipment as shown in Figure 4-6.

(2) Set the TR4515 controls as follows:

CW	1.999992 GHz
Output Power	−5 dBm
Frequency STD Switch (Rear Panel)	EXT

(3) On the R3265/3271, press the [PRESET] key and set the R3265/3271 controls as follows:

Center Freq	2 GHz
Span	20 kHz

(4) On the R3265/3271, press the [MENU] key, [SWEEP MODE], [SINGLE SWP], [SINGLE SWP], the [PEAK] key and the MARKER [ON] key, [⊿ MKR].

(5) Set the TR4515 controls as follows:

CW	2.000008 GHz

(6) On the R3265/3271, press the [MENU] key, [SWEEP MODE], [SINGLE SWP], [SINGLE SWP] and the [PEAK] key.
Record the ⊿MARKER frequency reading as the Actual ⊿ MARKER Reading in Table 4-7.
The reading should be within the limits shown.

(7) Set the frequency of the TR4515, the center frequency and span of the R3265/3271 as shown in Table 4-7, and repeat steps (5) through (7).

(LOG Span Accuracy)

(8) On the R3265/3271, press the [PRESET] key and the [FREQ SPAN] key [LOG SPAN].

(9) Set the R3265/3271 controls as follows:

Start frequency	100 MHz
Stop frequency	1 GHz

(10) Set the TR4515 controls as follows:

CW	200 MHz

(11) On the R3265/3271, press the [MENU] key, [SWEEP MODE], [SINGLE SWP], [SINGLE SWP] and the [PEAK] key.
Record the MARKER frequency in Table 4-8 as the Actual Marker Reading. The reading should be within the limits shown.

(12) Set the frequency of the TR4515, the start and stop frequency of the R3265/3271 as shown in Table 4-8, and repeat steps (10) through (12).

Table 4-7 Frequency Span Accuracy

TR4515 1st Frequency	TR4515 2nd Frequency	R3265/R3271		⊿ Marker Reading		
		Center Frequency	Span Setting	Min.	Actual	Max.
1.999992 GHz	2.000008 GHz	2 GHz	20 kHz	15.2 kHz		16.8 kHz
1.999980 GHz	2.000020 GHz	2 GHz	50 kHz	38 kHz		42 kHz
1.999840 GHz	2.000160 GHz	2 GHz	400 kHz	304 kHz		336 kHz
1.9992 GHz	2.0008 GHz	2 GHz	2 MHz	1.52 MHz		1.68 MHz
1.9992 GHz	2.0008 GHz	2 GHz	2.01 MHz	1.552 MHz		1.648 MHz
1.998 GHz	2.002 GHz	2 GHz	5 MHz	3.88 MHz		4.12 MHz
1.996 GHz	2.004 GHz	2 GHz	10 MHz	7.76 MHz		8.24 MHz
1.992 GHz	2.008 GHz	2 GHz	20 MHz	15.52 MHz		16.48 MHz
1.98 GHz	2.02 GHz	2 GHz	50 MHz	38.8 MHz		41.2 MHz
1.96 GHz	2.04 GHz	2 GHz	100 MHz	77.6 MHz		82. 4 MHz
1.92 GHz	2.08 GHz	2 GHz	200 MHz	155.2 MHz		164.8 MHz
1.8 GHz	2.2 GHz	2 GHz	500 MHz	388 MHz		412 MHz
1.6 GHz	2.4 GHz	2 GHz	1 GHz	776 MHz		824 MHz
1.2 GHz	2.8 GHz	2 GHz	2 GHz	1.552 GHz		1.648 GHz
2.9 GHz	6.1 GHz	4.5 GHz	4 GHz	3.104 GHz		3.296 GHz
1.3 GHz	7.7 GHz	4.5 GHz	8 GHz	6.208 GHz		6.592 GHz
<R3271 ONLY>						
9.996 GHz	10.004 GHz	10 GHz	10 MHz	7.76 MHz		8.24 MHz
9.96 GHz	10.04 GHz	10 GHz	100 MHz	77.6 MHz		82.4 MHz
9.6 GHz	10.4 GHz	10 GHz	1 GHz	776 MHz		824 MHz
9.2 GHz	10.8 GHz	10 GHz	2 GHz	1.552 GHz		1.648 GHz
16.996 GHz	17.004 GHz	17 GHz	10 MHz	7.76 MHz		8.24 MHz
16.96 GHz	17.04 GHz	17 GHz	100 MHz	77.6 MHz		82.4 MHz
16.6 GHz	17.4 GHz	17 GHz	1 GHz	776 MHz		824 MHZ
16.2 GHz	17.8 GHz	17 GHz	2 GHz	1.552 GHz		1.648 GHZ
8 GHz	12 GHz	10 GHz	5 GHz	3.88 GHz		4.12 GHZ
6 GHz	14 GHz	10 GHz	10 GHz	7.76 GHz		8.24 GHZ
2 GHz	18 GHz	10 GHz	19 GHz	15.52 GHz		16.48 GHZ

Table 4-8 LOG Span Accuracy

TR4515 Frequency	R3265/R3271		Marker Reading		
	Start Frequency	Stop Frequency	Min.	Actual	Max.
200 MHz	100 MHz	1 GHz	179MHz		221 MHz
500 MHz	100 MHz	1 GHz	449 MHz		551 MHz
800 MHz	100 MHz	1 GHz	719 MHz		881 MHz
20 MHz	10 MHz	1 GHz	17 MHz		23 MHz
50 MHz	10 MHz	1 GHz	44 MHz		56 MHz
80 MHz	10 MHz	1 GHz	71 MHz		89 MHz
100 MHz	10 MHz	1 GHz	89 MHz		111 MHz
200 MHz	10 MHz	1 GHz	179 MHz		221 MHz
500 MHz	10 MHz	1 GHz	449 MHz		551 MHz
800 MHz	10 MHz	1 GHz	719 MHz		881 MHz
10 MHz	1 MHz	1 GHz	8 MHz		12 Mhz
20 MHz	1 MHz	1 GHz	17 MHz		23 MHz
50 MHz	1 MHz	1 GHz	44 MHz		56 MHz
80 MHz	1 MHz	1 GHz	71 MHz		89 MHz
100 MHz	1 MHz	1 GHz	89 MHz		111 MHz
200 MHz	1 MHz	1 GHz	179 MHz		221 MHz
500 MHz	1 MHz	1 GHz	449 MHz		551 MHz
800 MHz	1 MHz	1 GHz	719 MHz		881 MHz

4.4.7 Resolution Bandwidth Accuracy and Selectivity

- SPECIFICATION

Range:	10 Hz to 3 MHz; 1, 3, 10 Sequence
Accuracy:	±50% (Resolution Bandwidth 10 Hz to 100 Hz, Digital IF) ±15% (Resolution Bandwidth 10 Hz to 1 MHz) ±25% (Resolution Bandwidth 3 MHz, 30 Hz) Note: 30 Hz at 25°C ± 10°C
Selectivity:	<15:1 (100 Hz to 3 MHz) <20:1 (30 Hz) 5 : 1 (10 Hz to 100 Hz, Digital IF) Nominal
Bandwidth (6 dB):	200 Hz, 9 kHz and 120 kHz (based on CISPR specifications)

- RELATED ADJUSTMENT

- DESCRIPTION
  This test measures the resolution bandwidth accuracy and selectivity. The 60 dB bandwidth is then determined and the results used to calculate the selectivity for each bandwidth (Selectivity = 60 dB BW/3 dB BW).

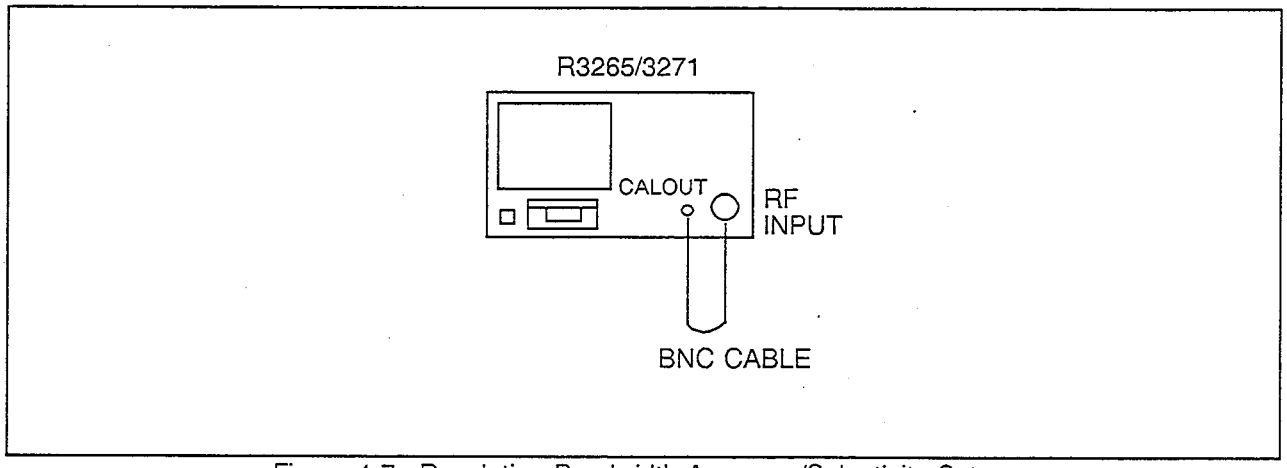


Figure 4-7 Resclution Bandwidth Accuracy/Selectivity Setup

- PROCEDURE

[Resolution Bandwidth Accuracy]

(1) Connect the R3265/3271 CALOUT to the INPUT 50 Ω as shown in Figure 4-7.

(2) Press [PRESET] and set the controls as follows:

Press [CENTER] [2] [5] [MHz] .

Press [FREQ SPAN] [5] [MHz] .

Press [PEF LEVEL] [5] [-dBm] and [dB/div] [1] [dB] .

Press [CPL] [RBW] [3] [MHz] .

Press [CPL] [NEXT MENU] [DIGTAL IF 1/2/OFF] [DIGTAL IF 1/2/OFF] to set Digital IF to "OFF".

Press [MENU] [TRACE DET] [SAMPLE] .

(3) Press [PEAK] , MARKER [ON] [dB DOWN] [x dB DOWN] and set [CONT DOWN ON/OFF] to ON.

(4) Press [MENU] [SWEEP MODE] [SINGLE SWP] , [SINGLE SWP] and wait for a new sweep to finish.

(5) Record the marker frequency in Tables 4-9 and 4-10 as actual 3 dB bandwidth.

(6) Change the RBW and span frequency as shown in Table 4-9, and repeat steps 4 and 5 for remaining RBWs.

Note : For measure RBW 100Hz to 10Hz, press the [CPL] key [NEXT MENU] and [DIGTAL IF 1/2/OFF] set Digital IF to "1".

[Resolution Bandwidth Selectivity]

(7) Press [PRESET] and set the controls as follows:

Press [CENTER FREQ] [2] [5] [MHz] .

Press [FREQ SPAN] [2] [5] [MHz] .

Press [CPL] [RBW] [3] [MHz] .

Press [VBW] [1] [0] [kHz] .

Press [CPL] key [NEXT MENU] and [DIGTAL IF 1/2/OFF] twice to set Digital IF to "OFF".

Press [MENU] [TRACE DET] [SAMPLE] .

(8) Press [PEAK], MARKER [ON] [dB DOWN], set [x dB DOWN] 60 dB and [CONT DOWN ON/OFF] to ON.

(9) Press [MENU] [SWEEP MODE] [SINGLE SWP], [SINGLE SWP] and wait for a new sweep to finish.

(10) Record the marker frequency in Table 4-10 as actual 60 dB bandwidth.

(11) Divide the 60 dB bandwidth by the 3 dB bandwidth and record as the Actual Resolution Bandwidth Selectivity in Table 4-10.

(12) Change the RBW and span frequency as shown in Table 4-10, and repeat steps (9) through (11) for remaining RBWs.
(For 10 Hz RBW, digital IF, set averaging to ten times because of close noise sidebands involved.
Press [MENU] [SWEEP MODE] [CONT SWP], [A] [AVG A] [1] [0] [Hz] .)
Set VBW to AUTO if RBW is 10kHz or below.

Table 4-9 Resolution Bandwidth Accuracy

Resolution Bandwith Setting	Frequency Span Setting	3dB Bandwidth		
		Min.	Actual	Max.
3 MHz	5 MHz	2.25 MHz		3.75 MHz
1 MHz	2 MHz	850 kHz		1.15 MHz
300 kHz	500 kHz	255 kHz		345 kHz
100 kHz	200 kHz	85 kHz		115 kHz
30 kHz	50 kHz	25.5 kHz		34.5 kHz
10 kHz	20 kHz	8.5 kHz		11.5 kHz
3 kHz	5 kHz	2.55 kHz		3.45 kHz
1 kHz	2 kHz	850 Hz		1150 Hz
300 Hz	500 Hz	255 Hz		345 Hz
100 Hz	200 Hz	85 Hz		115 Hz
(*1)30 Hz	200 Hz	22.5 Hz		37.5 Hz
100 Hz, Digital IF	200 Hz	50 Hz		150 Hz
30 Hz, Digital IF	200 Hz	15 Hz		45 Hz
10 Hz, Digital IF	200 Hz	5 Hz		15 Hz

*1: The MIN and MAX values for RBW 30 Hz are those when the temperature is 25°C ± 10°C. Values for other temperature range are not specified.

Table 4-10 Resolution Bandwidth Selectivity

Resolution Bandwith Setting	Frequency Span Setting	60 dB Bandwidth	3 dB Bandwidth	Selectivity	
				Actual	Max.
3 MHz	25 MHz				15
1 MHz	20 MHz				15
300 kHz	5 MHz				15
100 kHz	1 MHz				15
30 kHz	500 kHz				15
10 kHz	200 kHz				15
3 kHz	50 kHz				15
1 kHz	20 kHz				15
300 Hz	5 kHz				15
100 Hz	2 kHz				15
30 Hz	1 kHz				20
100 Hz, Digital IF	1 kHz				5 (nominal)
30 Hz, Digital IF	500 Hz				5 (nominal)
10 Hz, Digital IF	200 Hz				5 (nominal)

4.4.8 Resolution Bandwidth Switching Uncertainty

- SPECIFICATION

  100 Hz to 3 MHz RZSBW: < ±0.3 dB (referred to 300 kHz RES BW)

  30 Hz RESBW: < ±1 dB

  Digital IF:

  10 Hz to 100 Hz < 1.5 dB

- RELATED ADJUSTMENT
  There is no related adjustment procedure for this performance test.

- DESCRIPTION
  This test utilizes the CALOUT signal for measuring the switching uncertainty between resolution bandwidths. At each resolution bandwidth setting, the displayed amplitude variation of the signal in measured. All measurements are referenced to the 300 kHz bandwidth.

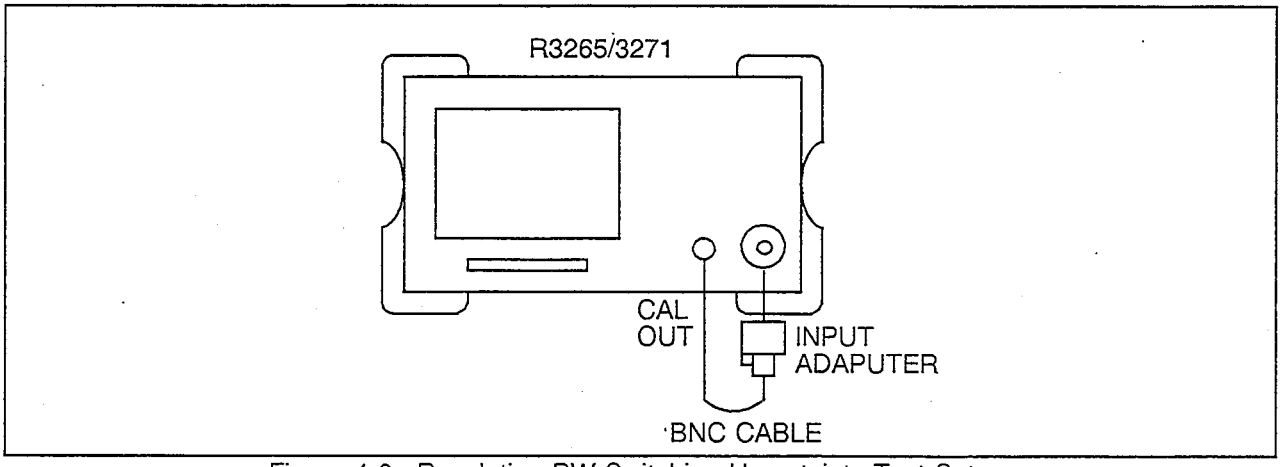


Figure 4-8 Resolution BW Switching Uncertainty Test Setup

- EQUIPMENT

  Adapters :
  Typed N(m) to BNC (f) . . . . . JCF-AF 001E×3

  Cables:
  BNC 10 cm MC-61

- PROCEDURE

(1) Connect the R3265/3271 CALOUT to the INPUT 50 Ω as shown in Figure 4-8.

(2) Press the [PRESET] key, the [SHIFT] key and the [CAL 7] key [EACH ITEM] [RBW SWITCH].

Wait for the "Calibration in progress" message to disappear then press the [CPL] key, [NEXT MENU], [DIGTAL IF 1/2/OFF] [DIGTAL IF 1/2/OFF] to set the Digital IF to "OFF".

Set the instrument controls as follows:

Center Freq	25 MHz
Span	1 MHz
Ref Level	−5 dBm
RBW	300 kHz
Sweep Mode	SINGLE
dB/Div	1 dB

(3) Press the [MENU] key, [SWEEP MODE] [SINGLE SWP], the [PEAK] key and the MARKER [ON] key, [⊿MKR] [FIXED MKR ON/OFF].

(4) Set the frequency span and RBW to the values listed in the second entry of Table 4-11 (Span 5 MHz, RBW 3 MHz).

(5) Press the [MENU] key, [SWEEP MODE] [SINGLE SWP] and the [PEAK] key,

Record the ⊿MARKER amplitude in the Actual⊿ MARKER Reading column of Table 4-11. The MARKER reading should be within the limit shown.

CAUTION

Press the [CPL] key [NEXT MENU] and [DIGTAL IF 1/2/OFF] set Digital IF to "1" when measuring the resoution BW switching uncertainty of digital IF.

(7) Repeat steps 4 and 5 for each set of frequency span and RBW settings in Table 4-11.

Table 4-11 Resolution BW Switching Uncertainty

R3265/R3271		⊿ Marker Reading		
Span	RBW	Min. (dB)	Actual	Max. (dB)
1 MHz	300 kHz	0	0 (Ref.)	0
5 MHz	3 MHz	−0.3		+0.3
2 MHz	1 MHz	−0.3		+0.3
200 kHz	100 kHz	−0.3		+0.3
50 kHz	30 kHz	−0.3		+0.3
20 kHz	10 kHz	−0.3		+0.3
5 kHz	3 kHz	−0.3		+0.3
2 kHz	1 kHz	−0.3		+0.3
500 Hz	300 Hz	−0.3		+0.3
200 Hz	100 Hz	−0.3		+0.3
200 Hz	30 Hz	−1		+1
200 Hz	*100 Hz	−1.5		+1.5
200 Hz	*30 Hz	−1.5		+1.5
200 Hz	*10 Hz	−1.5		+1.5

*: Digital IF

4.4.9 Displayed Average Noise Level

- SPECIFICATIONS

  Displayed Average Noise level: Resolution bandwidth 10 Hz, input attenuator 0 dB, video bandwidth 1 Hz.

(R3265)

Frequency range	Average Noise Level
1 kHz	−100 dBm
10 kHz	−110 dBm
100 kHz	−111 dBm
1 MHz	−135 dBm
10 MHz to 3.6 GHz	−{140−1.55×f(GHz)} dBm −{145−1.55×f(GHz)} dBm (Low noise mode)
3.5 GHz to 8 GHz	−135 dBm

(R3271)

Frequency range	Average Noise Level
1 kHz	−100 dBm
10 kHz	−110 dBm
100 kHz	−111 dBm
1 MHz to 3.6 GHz	−{135−1.55×f(GHz)} dBm
3.5 GHz to 7.5 GHz	−130 dBm
7.5 GHz to 15.4 GHz	−123 dBm
15.2 GHz to 23.3 GHz	−116 dBm
23 GHz to 26.5 GHz	−110 dBm

- RELATED ADJUSTMENT

  Frequency response adjustment.

- DESCRIPTION

  This test measures the displayed average noise level in all frequency tests. The analyzer's input is terminated at 50 Ω. In Band 1, in the frequence range from 100 Hz to 3.6 GHz, the test first measures the average noise at 1 kHz, 10 kHz, 100 kHz and 1000 kHz, then at any frequency point in zero span. For the rest of Band 1, and for all remaining bands, the test tunes the analyzer frequency across the band, uses the marker to locate the frequency with the highest response, and then reads the average noise in zero span. In the case of the R3265 only, a LOW NOISE function is provided, so the test measures the average noise level at 25 MHz when the LOW NOISE function is set to ON.

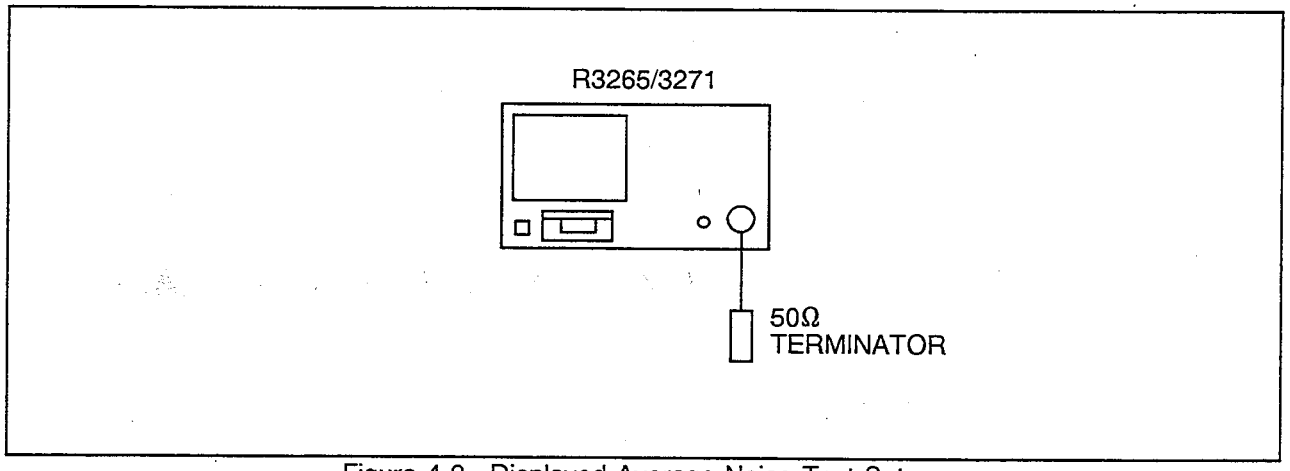


Figure 4-9 Displayed Average Noise Test Setup

- EQUIPMENT

  50 Ω Terminator

- PROCEDURE

[Displayed Average Noise, Band 1]

(1) Connect the eqiptment as shown in Figure 4-9.
Press [PRESET] and set the controls as follows:

Center Frequency	1 kHz
Span Frequency	0 Hz
Reference Level	−60 dBm
Resolution Bandwidth	30 Hz
Digital IF	OFF
Video Bandwidth	1 Hz
Input Attenuator	0dB

(2) Press [A] [AVG A] [1] [0] [Hz] and wait for averaging to finish and press [PEAK] .

(3) Read the marker level and record it in Table 4-12 as the Displayed Noise Level at 1kHz.

(4) Press [PRESET] and set the controls as follows:

Center Frequency	10 kHz
Span Frequency	0 Hz
Reference Level	−60 dBm
Input Attenuator	0 dB
Resolution Bandwidth	300 Hz
Video Bandwidth	1 Hz
Sweep Time	500 msec

(5) Press [MENU] [SWEEP MODE] [SINGLE SWP] and wait for a new sweep to finish,

then press [PEAK] .

(6) Read the marker level and record it in Table 4-12 as the Displayed Noise Level at 10 kHz.

(7) Change the center frequency to each of the values listed in column 1 of Table 4-12 and repeat step 5 sequentially. Read the marker level and record it in Table 4-12 as the Displayed Noise level at Center Frequency.

(8) Press [PRESET] and set the controls as follows:

Start Frequency	3.501 GHz
Stop Frequency	8 GHz (7.5 GHz for R3271)
Reference Level	−40 dBm
Resolution Bandwidth	3 MHz
Video Bandwidth	100 kHz
Input Attenuator	0 dB

(9) Press [A] [AVG A] [1] [0] [Hz] and wait for averaging to finish.

(10) Press [PEAK], [MKR→] [MKR→CF] and [A] [WRITE A].

(11) Set the controls as follows:

Span Frequency	0 Hz
Reference Level	−60 dBm
Resolution Bandwidth	300 Hz
Video Bandwidth	1 Hz
Sweep Time	500 msec

(12) Press [MENU] [SWEEP MODE] [SINGLE SWP] [SINGLE SWP] and [PEAK].

(13) Read the marker level and record it in Table 4-12 as the Displayed Average Noise Level from 3.5 GHz to 8 GHz (7.5 GHz for R3271).

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[Displayed Average Noise Level, Band 2 (R3271 only)]

(14) Press PRESET and set the controls as follows:

Start Frequency	7.501 GHz
Stop Frequency	15.4 GHz
Reference Level	−40 dBm
Resolution Bandwidth	3 MHz
Video Bandwidth	100 kHz
Input Attenuator	0 dB

(15) Repeat steps (9) through (12).

(16) Read the marker level and record it in Table 4-12 as the Displayed Noise level from 7.5 GHz to 15.4 GHz.

[Displayed Average Noise, Band 3 (R3271 only)]

(17) Press PRESET and set the controls as follows:

Start Frequency	15.201 GHz
Stop Frequency	23.3 GHz
Reference Level	−40 dBm
Resolution Bandwidth	3 MHz
Video Bandwidth	100 kHz
Input Attenuator	0 dB

(18) Repeat steps (9) through (12).

(19) Read the marker level and record it in Table 4-12 as the Displayed Average Noise Level from 15.2 GHz to 23.3 GHz.

[Displayed Average Noise, Band 4 (R3271 only)]

(20) Press [PRESET] and set the controls as follows:

Start Frequency	23.001 GHz
Stop Frequency	26.5 GHz
Reference Level	−40 dBm
Resolution Bandwidth	3 MHz
Video Bandwidth	100 kHz
Input Attenuator	0 dB

(21) Repeat steps (9) through (12).

(22) Read the marker level and record it in Table 4-12 as the Displayed Average Noise Level from 23 GHz to 26.5 GHz.

[Displayed Average Noise at 25 MHz when setting the LOW NOISE function On. (R3265 only)]

(23) Press [PRESET] and set the R3265 controls as follows:

Press [REF LEVEL] and [LOW NOISE ON/OFF] set LOW NOISE to "ON".

Center Frequency	25 MHz
Span Frequency	200 Hz
Resolution Bandwidth	10 Hz (Digital IF)
Input Attenuator	0 dB
REF LEVEL	-90dBm

(24) Press [A] [AVG A] [5] [0] [Hz] and wait for averaging to finish.

(25) Press [PEAK] and read the marker level and record it as Maximum Low Noise.

Press [PEAK] [MIN] and read the marker level and record it as Minimum Low Noise.

(26) Displayed Average Noise in LOW NOISE mode is provided:

$$\text{LOW NOISE} = \frac{(\text{Maximum Low Noise} + \text{Minimum Low Noise})}{2} \text{ (dBm)}$$

Record the result as the LOW NOISE in Table 4-12.

Table 4-12 Displayed Average Noise Level (R3265)

Frequency	Displayed Average Noise Level (dBm)	Specification (dBm)
1 kHz		−95.23
10 kHz		−95.23
100 kHz		−96.23
1.1 MHz		−120.23
10.1 MHz		−125.21
101 MHz		−125.07
501 MHz		−124.45
1001 MHz		−123.68
1.5 GHz		−122.90
2.0 GHz		−122.13
2.5 GHz		−121.35
3.0 GHz		−120.58
3.5 GHz		−119.80
3.5 GHz to 8 GHz		−120.23
24 MHz (LOW NOISE)		−145.0

Table 4-13 Displayed Average Noise Level (R3271)

Frequency	Displayed Average Noise Level (dBm)	Specification (dBm)
1 kHz		−95.23
10 kHz		−95.23
100 kHz		−96.23
1.1 MHz		−120.23
10.1 MHz		−120.21
101 MHz		−120.07
501 MHz		−119.45
1001 MHz		−118.68
1.5 GHz		−117.90
2.0 GHz		−117.13
2.5 GHz		−116.35
3.0 GHz		−115.58
3.5 GHz		−114.80
3.5 GHz to 7.5 GHz		−115.23
7.5 GHz to 15.4 GHz		−108.23
15.2 GHz to 23.3 GHz		−101.23
23 GHz to 26.5 GHz		−95.23

4.4.10 Gain Compression

- SPECIFICATION

R3265: —5 dBm (mixer level) > 200 MHz
—10 dBm (mixer level) > 10 MHz

R3271: —5 dBm (mixer level) > 10 MHz

- RELATED ADJUSTMENT
  There is no related adjustment procedure for this performance test.

- DESCRIPTION
  This test means gain compression in the low and high bands.
  Two signals, separated by 1 MHz, are used. First a —30 dBm signal is placed at the input of the R3265/3271.
  After that, input a signal at —5 dBm or above and increase its signal level. The initial signal level at —30 dBm is lowered. Measure the input level when the signal is lowered by 1 dB.

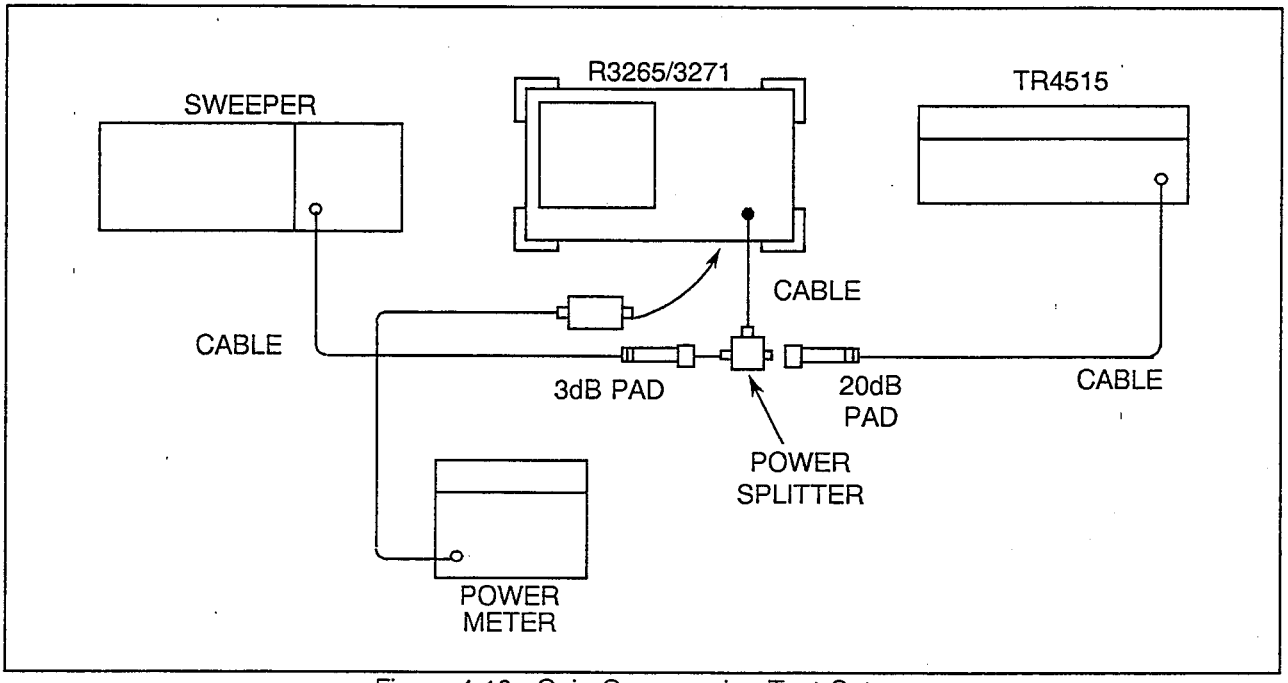


Figure 4-10 Gain Compression Test Setup

- EQUIPMENT

Synthesized Sweeper	TR4515
Sweeper	HP8350 + HP83595A
Power Meter	HP436A
Power Sensor	HP848/A
Power Splitter	Model 1579
20 dB Pad	DEE-000480-1
3 dB Pad	DEF-000685-1
Cable: SMA (3 required)	

- PROCEDURE

(1) Zero and calibrate the power meter.

(2) Connect the equipment as shown in Figure 4-10.

(3) Press the INSTR PRESET by on both the TR4515 and the sweeper.
Set the controls for the HP8350 as follows:

CW	11 MHz
CW Filter	ON
Power Level	−2 dBm

(4) Set the controls for the TR4515 as follows:

CW	10 MHz
Power Level	−4 dBm

(5) On the R3265/3271, press the [PRESET] key.
Set the R3265/3271 controls as follows:

Center Freq	10.5 MHz
Span	20 MHz
ATT	0 dB
dB/div	1 dB/div

(6) On the HP8350, press the vernier key.
Turn the vernier knob of the HP8350 so that the displayed signal on the R3265/3271 screen enters the range within ±2 div. from the center on the horizontal axis.
On the R3265/3271, press [SPAN] and [↓] .
Turn the vernier knob of the HP8350 so that the displayed signal on the R3265/3271 screen enters the range within ±1 div. from the center on the horizontal axis.
On the R3265/3271, press [SPAN] and [↓] .
Turn the vernier knob of the HP8350 so that the displayed signal on the R3265/3271 screen enters the range within ±1 div. from the center on the horizontal axis.
On the R3265/3271, press [SPAN] and [↓] .
Turn the vernier knob of the HP8350 so that the displayed signal on the R3265/3271 screen enters the range of 2.5 div.±0.5 div. on the right side of the center on the horizontal axis.
Now, the frequency of the HP8350 output signal is set to 11 MHz ± 0.1 MHz.

(7) On the R3265/3271, set the [REF LEVEL] to −30 dBm.

(8) On the HP8350, press the [RF] key to set the output to OFF.

(9) Adjust the power level of the TR4515 for a displayed signal level of −30 dBm ± 0.1 dB on the R3265/3271 screen.

(10) On the HP8350, press the [RF] key to set the output to ON.

(11) Turn the power level knob on the HP8350 until the signal level at 2.5 div. in the lefthand part on the R3265/3271 screen is lowered by 1 dB from −30 dBm. If the power level knob cannot be turned any more, stop it there.

(12) Remove the SMA cable from the input terminal of the R3265/3271 and connect the power sensor there.

(13) Record the amplitude reading on the power meter.
It should be greater than −5 dBm (R3265: −10 dBm)

_____ dBm

Steps 14 through 18 are not necessary for the R3271.

(14) Set the HP8350 controls as follows:

CW ..... 200 MHz

(15) Set the TR4515 controls as follows:

CW	200 MHz

(16) Set the R3265 controls as follows:

Center Freq	200.5 MHz
Span	20 MHz
Ref Level	−10 dBm

(17) Repeat steps (6) through (12).

(18) Record the amplitude reading on the power meter.
It should be greater than −5 dBm.

The following steps are to be performed for both the R3265 and R3271.

(19) Rotate the CAL FACTOR switch to the power sensor's 3.6 GHz calibration factor.

(20) Set the HP8350 controls as follows:

CW	3.6 GHz
Power Level	-2dBm

(21) Set the TR4515 controls as follows:

CW	3.6 GHz

(22) Set the R3265/3271 controls as follows:

Center Freq	3.6005 GHz
Span	20 MHz
Ref Level	−10 dBm
dB/div	10 dB

(23) On the R3265/3271, press MARKER [ON] [NEXT MENU] [PRESELE] [PEAK SEARCH], [AUTO PEAKING].

Wait for the "peaking!!" message to disappear.
Set the dB/div to 1dB/div.

(24) Repeat steps (6) through (12).

(25) Record the amplitude reading on the power meter.
It should be greater than −5 dBm.

_____ dBm

Table 4-14 Gain Compression

R3265/71 Center Freq (MHz)	TR4515 CW (MHz)	HP8350 CW (MHz)	1dB Gain Compression level (dBm)
10.5	10	11	
200.5	200	201	
3600.5	3600	3601	

4.4.11 Residual Response

- SPECIFICATION

R3265:
- 1 MHz to 3.6 GHz < – 100 dBm (with no signal at input and 0 dB input attenuation)
- 300 kHz to 8 GHz < – 90 dBm

R3271:
- 1 MHz to 3.6 GHz < – 100 dBm
- 300 kHz to 8 GHz < – 90 dBm

- RELATED ADJUSTMENT

There is no related adjustment for this performance test.

- DESCRIPTION

This test checks for residual responses. Any response located above the display line is measured in a narrow frequency span and resolution bandwidth. The RF INPUT is terminated in 50 Ω.

- EQUIPMENT

Coaxial 50 Ω Termination

Adapters:

Type N to SMA HRM-554s

Type N to BNC

Cable:

BNC, 150cm MI-09

- PROCEDURE

(1) On the R3265/3271, press the PRESET key and set the controls as follows;

Center Freq	25 MHz
Span	10 kHz
Ref Level	– 10 dBm
RES BW	300 Hz
ATT	0 dB

(2) Connect a BNC cable between the CAL OUTPUT and the RF INPUT and press the [PEAK] Key.

Check that the marker amplitude is within -10.0 dBm ±0.2 dB. If it is out of the range, press [SHIFT], [CAL 7] and [CALL ALL]. Then, red-check that the marker amplitude is within −10.0 dBm ±0.2 dB.

<<Residual Responses, base band>>

(3) Remove the BNC cable and adapter from the RF INPUT.

Install the Type N to SMA adapter and 50 Ω termination on the RF INPUT. Press the [PRESET] key and set the controls as follows:

Center Freq	1.3 MHz
Span	2 MHz
CF Step	1.9 MHz
Ref Level	−50 dBm
ATT	0 dB
RES BW	10 kHz
Video BW	300Hz

(4) Press [MENU] key [DSP LINE ON/OFF] and [1] [0] [0], [-dBm] key.

Press [MENU] key [SWEEP MODE] and [SINGLE SWP].

The noise level should be at least 3 dB below the display line. If it is not, it will be necessary to reduce the Span and RES BW to reduce the noise level.

If the Span is reduced, reduce the CF Step to no more than 95 % of the Span.

(5) If a residual is suspected, press [SINGLE SWP] again. A residual response will persist, but a noise peak will not. Record the frequency and amplitude of any responses above the display line.

(6) If a response is marginal, verify the response amplitude as follows:

① Press the [SHIFT] and [SAVE / RECALL] key, [1], [Hz] key, [SAVE / EXECUTE].

② Press the [MENU] key, [SWEEP / MODE], [CONT / SWP].

③ Place the marker on the peak of the response in question.

④ Press the [MKR→] key, [MKR→CF].

⑤ Press the [CPL] key, [RBW], [AUTO].

⑥ Continue to reduce the Span until a RES BW of 300 Hz is reached.

Press [PEAK] [MKR→] [MKR→CF] set peak to center.

⑦ Record the frequency and amplitude of any residual response above the display line.

⑧ Press the [RECALL] key, [RECALL / EXECUTE].

(7) Check for residuals up to 3.599 GHz using the procedure of step (4) through (6) above. To change the center frequency, then press the [CENTER FREQ] and [↑] keys.

<<Residual Response, 3.5 to 7.5 GHz Band>>

(8) Set the R3265/3271 as follows:

Center Freq	3.625 GHz
Span	50 MHz
CF Step	47.5 MHz
RES BW	300 kHz
Video BW	300 Hz

Press the [MENU] key, [DSP LINE / ON/OFF] [9] [0] [-dBm] key.

(9) Check for residuals up to center frequency 7.425GHz using the procedure of steps (4) through (6) above. To change the center frequency, then press the [CENTER FREQ] and [↑] keys.

Lastly check for residuals at center frequency 7.475GHz using the procedure of steps (4) through (6) above.

4.4.12 Second Harmonic Distortion

- SPECIFICATION

R32655:
- −70 dBc (100 MHz to 3.6 GHz, −30 dBm mixer level)
- −60 dBc (10 MHz to 3.6 GHz, −30 dBm mixer level)
- −100 dBc (>3.6 GHz, −10 dBm mixer level)

R32715:
- −70 dBc (10 MHz to 3.6 GHz, −30 dBm mixer level)
- −100 dBc (>3.6 GHz, −10 dBm mixer level)

- RELATED ADJUSTMENT

There is no related adjustment procedure for the performance test.

- DESCRIPTION

A synthesized sweeper and low-pass filter provide the signal for measuring second harmonic distortion. The low-pass filter eliminates any harmonic distortion originating at the signal source. The R3265/3271 frequency response is calibrated. The synthesized sweeper is phase-locked to the spectrum analyzer's 10 MHz reference.

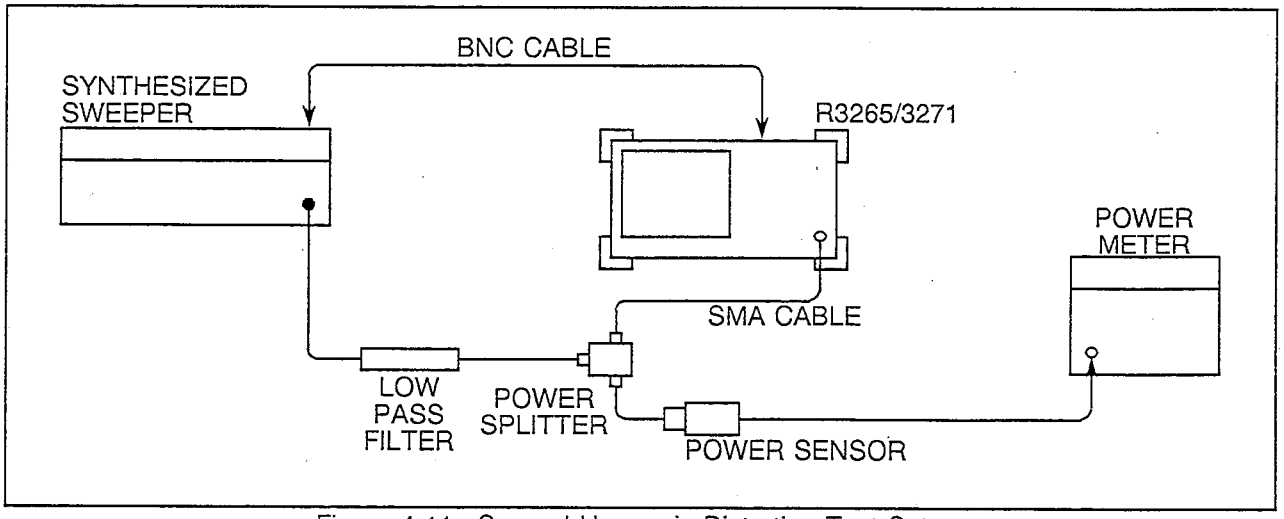


Figure 4-11 Second Harmonic Distortion Test Setup

- EQUIPMENT

Synthesized Sweeper	TR4515
Power Meter	HP436A
Power Sensor	HP8485A or HP8481A
Power Splitter	Model 1579
2 GHz Low-pass Filter	DEE-001172-1
Adapter:	
Type N to SMA	HRM-554S
Cables:	
BNC, 150 cm	MI-09
SMA, 70 cm	A01002

- PROCEDURE

[100 Hz to 3.6 GHz Band]

(1) Zero and calibrate the power meter. Rotate the CAL FACTOR switch to the power sensor's 1.5 GHz calibration factor.

(2) Connect the equipment as shown in Figure 4-11.

(3) Press the [INSTR PRESET] key on the TR4515. Set the TR4515 controls as follows:

CW	1.5 GHz
Power Level	0 dBm
Frequency Standard Switch (rear panel)	EXT 10 MHz

(4) On the R3265/3271, press [PRESET] and set the controls as follows:

Center Freq	1.5 GHz
Span	10 kHz
VBW	30 Hz
ATT	20 dB
Ref Level	−10 dBm

(5) Set the TR4515 [POWER LEVEL] key for a -10 dBm ± 0.1 dB reading on the power meter.

(6) On the R3265/3271, press [MENU] [SWEEP MODE] [SINGLE SWP], [PEAK], MARKER [ON] [MKR] [FIXED MKR ON/OFF].

(7) On the R3265/3271, press [CENTER FREQ] [3] [GHz], [MENU] [SWEEP MODE] [SINGLE SWP].
Wait for completion of the sweep.
Press [PEAK] and record the amplitude of [MKR].
It should be less than -70 dBc.

Second Harmonic Distortion (<3.6 GHz)_____dBc

[>3.6 GHz Band]

(8) Remove the low-pass-filter and connect an SMA cable between the TR4515 and the R3265/3271.

(9) On the R3265/3271, press [PRESET] and set the controls as follows:

Center Freq	3.8 GHz
Span	500 kHz

(10) Set the TR4515 controls as follows:

CW	3.8 GHz
Power Level	−10 dBm

(11) On the R3265/3271, press MAKER [ON] [NEXT MENU] [PRESELE] [PEAK SEARCH] [AUTO PEAKING].
Wait for the "peaking" message to disappear.

(12) Set the TR4515 controls as follows:

CW	1.9 GHz
Power Level	0 dBm

(13) Connect the equipment as shown in Figure 4-11.

(14) Rotate the CAL FACTOR switch to the power sensor's 1.9 GHz calibration factor.

(15) Set the TR4515 [POWER LEVEL] key for a 0 dBm ±0.1 dB reading on the power meter.

(16) Set the R3265/3271 center frequency to 1.9 GHz and span to 1 kHz.

Press [PEAK] MAKER [ON] [⊿ MKR] [FIXED MKR ON/OFF] .

Set the center frequency to 3.8 GHz and ref-level to -40 dBm.

Press [A] [AVG A] [2] [0] [Hz] .

Wait for the end of 20 averagings.

Press [PEAK] and record the ⊿ MKR amplitude.

It should be less than – 100 dBc

Second Harmonic Distortion (>3.6 GHz)_____dBc

4.4.13 Third Order Intermodulation Distortion

- SPECIFICATION

For a total mixer input level* of -30 dBm:

R3265	R3271
10 MHz to 3.6 GHz : < – 60 dBc 200 MHz to 3.6 GHz : < – 70 dBc 3.5 GHz to 8 GHz : < – 75 dBc	10 MHz to 3.6 GHz : – 70 dBc 3.5 GHz to 26.5 GHz : < – 75 dBc

* Total mixer input level = Total Input Level - Input Attenuation

Converted Specification for a total mixer input level* of -20dBm:

R3265	R3271
10 MHz to 3.6 GHz : < – 40 dBc 200 MHz to 3.6 GHz : < – 50 dBc 3.5 GHz to 8 GHz : < – 55 dBc	10 MHz to 3.6 GHz : < – 50 dBc 3.5 GHz to 26.5 GHz : < – 55 dBc

- RELATED ADJUSTMENT

There is no related adjustment procedure for this performance test.

- DESCRIPTION

Two synthesized sweepers provide the signals required for measuring third order intermodulation.

It is difficult when the input level is low because of being buried to the noise, to measure the spectrum generated by the distortion. Third order intermodulation distortion is raised by 20dB if the input level is raised by 10dB.

Then, examine with mixer input level set in -20dBm after the spec is converted into a value which is 20dB larger.

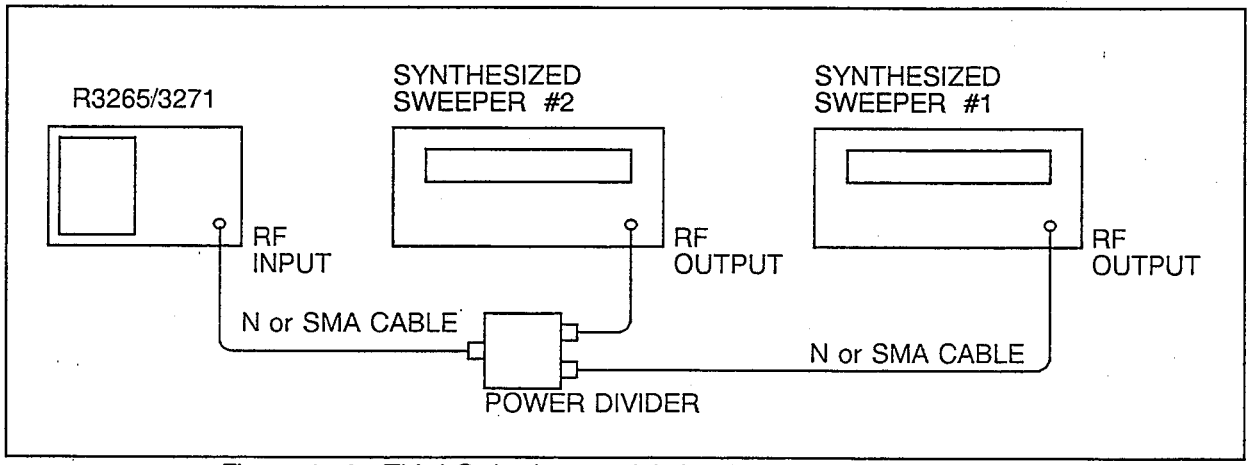


Figure 4-12 Third Order Intermodulation (<300 MHz) Test Setup

- EQUIPMENT

Instrument	Critical Specifications for Equipment Substitutuion	Recommended Model
Synthesized Sweeper	Frequency Range: 10 MHz to 4 GHz Power Level: – 10 to 0 dBm	TR4515 R4262
Power Divider #1	Frequency Range: 10 MHz to 300 MHz Isolation: > 20 dB	H-8-4 (ANZAC)
Power Divider #2	Frequency Range: 1 GHz to 4 GHz	4313-2 (NARDA)

- PROCEDURE

The following procedure carryout at -20dBm for a total mixer input level.

[Third Order Intermodulation (<300 MHz)]

(1) Select power divider #1 and connect the units as shown in Figure 4-12.

(2) Press the [INSTR PRESET] key on each synthesized sweeper. Set each of the synthesized sweeper controls as follows:

Power Level	– 10 dBm
CW (synthesized sweeper #1)	10.5 MHz (205 MHz)
CW (synthesized sweeper #2)	10.6 MHz (205.1 MHz)
RF Out	OFF

(3) On the R3265/3271, press the [PRESET] key. Set the R3265/3271 controls as follows:

Center Freq	10.5 MHz (205 Mhz)
Ref Level	– 10 dBm
Freq Span	1 MHz
RBW	3 kHz
VBW	300 Hz
ATT	10 dB

(4) On the synthesized sweeper #1, set the [RF OUT] key to ON.

(5) On the R3265/3271, press the [PEAK] key, [NEXT MENU] and [CONT PK ON/OFF].

(6) On the synthesized sweeper #1, adjust the [POWER LEVEL] key for a −10 dBm ±0.1 dB reading on the R3265/3271 display.

(7) On the synthesized sweeper #1, set the [RF OUT] key to OFF. On the synthesized sweeper #2, set the [RF OUT] key to ON.

(8) On the synthesized sweeper #2, adjust the [POWER LEVEL] key for a -10 dBm ±0.1 dB reading on the R3265/3271 display.

(9) On the synthesized sweeper #1, set the [RF OUT] key to ON.

(10) On the R3265/3271, press the following keys: [CONT PK ON/OFF] and the [PEAK] key.

Wait for a new sweep to finish, then press the following keys: the [A] key, [VIEW A], the [PEAK] key, [ON] key and [⊿MKR].

(11) Third order intermodulation distortions appear symmetrically 100 kHz apart from the two carriers. Move ⊿ MKR to each distorted position with the knob or [↑] key, read the level in dBc and record the greater reading.

(12) For the R3271, only measurement with 10.5 MHz center frequency is made. For the R3265, repeat the steps for measurement with 205 MHz center frequency and record its result.

[Third Order Intermodulation, 3.6 GHz]

(13) Switch power divider #1 to #2.

(14) Press the [INSTR PRESET] key on each synthesized sweeper. Set each of the synthesized sweeper controls as follows:

Power Level	−10 dBm
CW (synthesized sweeper #1)	3.6 GHz
CW (synthesized sweeper #2)	3600.1 GHz
RF Out	OFF

(15) On the R3265/3271, press the PRESET key. Set the R3265/3271 controls as follows:

Center Freq	3.6 GHz
Ref Level	– 10 dBm
Span	1 MHz
(RBW)	3 kHz
(ATT)	10 dB
(VBW)	100 HZ

(16) Repeat steps (4) to (11) to measure the third order intermodulation distortions and record the greater reading.

Table 4-15 Third Order Intermodulation Distortion

(R3265)

Sythsized Sweeper #1 [CW] (MHz)	Sythsized Sweeper #2 [CW] (GHz)	Third Order Intermodulation Distortion	
		Actual (dBc)	Max (dBc)
10.5	10.6		-40
205	205.1		-50
3600	3600.1		-55

(R3271)

Sythsized Sweeper #1 [CW] (MHz)	Sythsized Sweeper #2 [CW] (GHz)	Third Order Intermodulation Distortion	
		Actual (dBc)	Max (dBc)
10.5	10.6		-50
3600	3600.1		-55

4.4.14 Image, Multiple and Out-of-Band Response

- SPECIFICATION

  Image, Multiple and Out-of-Band Response:

  R3265: – 70 dBc (10 MHz to 8 GHz)

  R3271: – 70 dBc (10 MHz to 18 GHz)
  – 60 dBc (10 MHz to 23 GHz)
  – 50 dBc (10 Mhz to 26.5 GHz)

- RELATED ADJUSTMENT
  YTF adjustment

- DESCRIPTION
  The performance tests in the R3265 and R3271 differ in measurement frequency. Make measurement with each band.

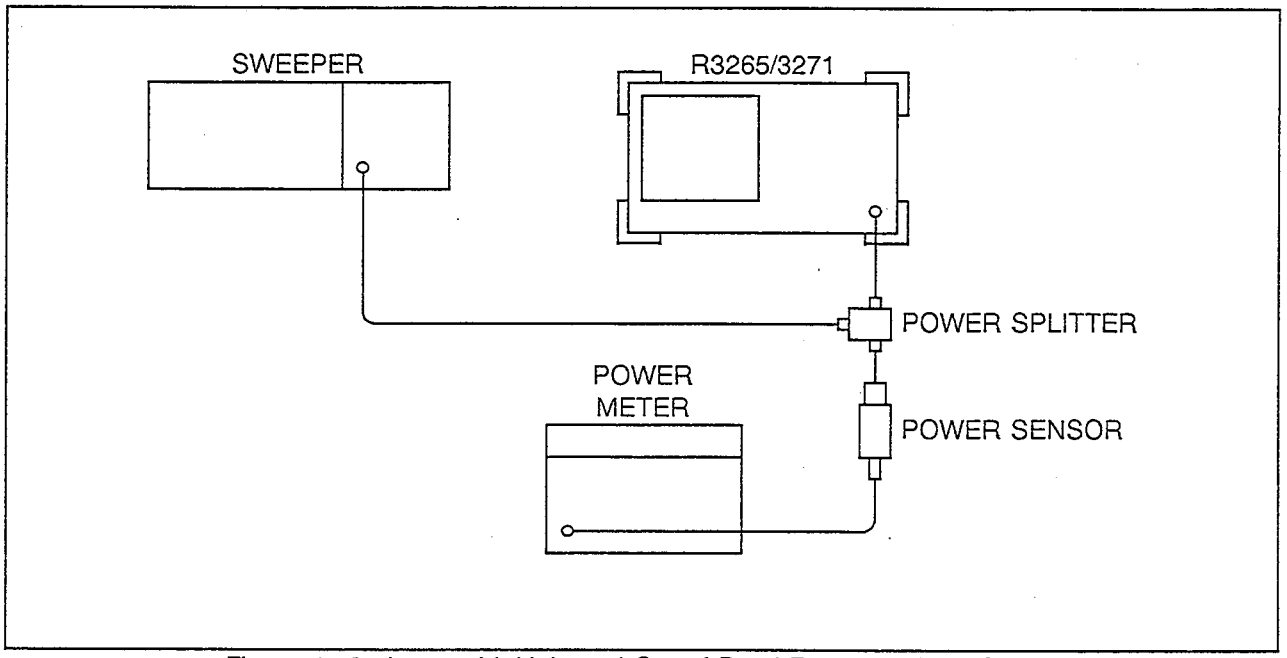


Figure 4-13 Image, Multiple and Out-of-Band Response Test Setup

- EQUIPMENT

Sweeper	HP8350 + HP83594A
Power Meter	HP436A
Power Sensor	HP8485A
Power Splitter	Model 1579
Adapter:	
Type N to SMA	HRM-554S
Cables:	
SMA, 70 cm	A01002

- PROCEDURE

[100 Hz to 3.6 GHz Band (R3265/3271)]

(1) Connect the equipment as shown in Figure 4-13, but do not connect the power sensor.

(2) Press the [INSTR PRESET] key on the sweeper and set the controls as follows:

CW	2 GHz
Power Level	0 dBm

(3) On the R3265/3271, press the [PRESET] key and set the controls as follows:

Center Freq	2 GHz
Span	40 MHz
RBW	100 kHz
VBW	300 Hz

(4) Zero and calibrate the power meter. Rotate the CAL FACTOR switch to the power sensor's 2 GHz calibration factor.
Connect the power sensor to the power splitter.

(5) Adjust the sweeper [POWER LEVEL] key for a 0 dBm ±0.1 dB reading on the power meter.
On the R3265/3271, press [PEAK] , [MKR→] , [MKR→CF] , [SPAN] [5] [MHz] [MENU]

(6) [SWEEP MODE] [SINGLE SWP] , [PEAK] MARKER [ON] [MKR] [FIXED MKR ON/OFF] [SPAN] [4] [0] [MHz] .

(7) For each of the frequencies listed in Table 4-16 (R3271) for the 100 Hz to 3.6 GHz band, do the following:

① Set the sweeper to the listed [CW] key frequency.

② On the power meter, rotate the CAL FACTOR switch to the appropriate power sensor calibration factor.

③ Set the sweeper [POWER LEVEL] key for a 0 dBm reading on the power meter.

④ Press [MENU] [SWEEP MODE] [SINGLE SWP] on the R3265/3271.

⑤ On the R3265/3271, press [PEAK] and record the ⊿MKR amplitude in Table 4-16 (R3271) as the response amplitude. The response amplitude should be less than the specification listed in the table.

(8) On the R3265/3271, press the MARKER [OFF], [MENU] [SWEEP MODE] [CONT SWP].

Measurement frequency for the R3265 is different for the following bands. Therefore, skip steps (9) to (27) and restart from step (28). The following steps are for the R3271.

[3.5 to 7.5 GHz Band (R3271 Only)]

(9) Set the R3271 center frequency to 5.5 GHz. Set the sweeper [CW] to 5.5 GHz.

(10) Rotate the CAL FACTOR switch to the power sensor's 5.5 GHz calibration factor on the power meter.

(11) On the sweeper, set the power level to the power meter indicate 0dBm.

On the R3271, press [PEAK] [MKR→] [MKR→CF], [SPAN] [5] [MHz], MARKER [ON] [NEXT MENU] [PRESELE] [PEAK SEARCH], [AUTO PEAKING]. Wait for the "peaking!!" message to disappear.

Press [MENU] [SWEEP MODE] [SINGLE SWP], [PEAK] MARKER [ON] [⊿ MKR] [FIXED MKR ON/OFF] [SPAN] [4] [0] [MHz].

(12) Repeat steps (7) and (8) for the sweeper frequencies listed in Table 4-16 for the 3.5 GHz to7.5 GHz band.

[7.4 GHz to 15.4 GHz Band (R3271 oNLY)]

(13) Set the R3271 center frequency to 12 GHz. Set the sweeper [CW] to 12 GHz.

(14) Rotate the CAL FACTOR switch to the power sensor's 12 GHz calibration factor on the power meter.

(15) Repeat step (11) for the R3271.

(16) Repeat steps (7) and (8) for the sweeper frequencies listed in Table 4-16 for the 7.4 GHz to 15.4 GHz band.

[15.2 GHz to 23.3 GHz Band (R3271 Only)]

(17) Set the R3271 [CENTER FREQ] to 21 GHz. Set the sweeper [CW] to 21 GHz.

(18) Rotate the CAL FACTOR switch to the power sensor's 21 GHz calibration factor on the power meter.

(19) Repeat step (11) for the R3271.

(20) Repeat steps (7) and (8) for the sweeper frequencies listed in Table 4-16 for the 15.2 to 23.3 GHz band.

[23 to 26.5 GHz Band (R3271 Only)]

(21) Set the R3271 center frequency to 24.4 GHz. Set the sweeper [CW] to 24.4 GHz.

(22) Rotate the CAL FACTOR switch to the power sensor's 24.4 GHz calibration factor on the power meter.

(23) Repeat step (11) for the R3271.

(24) Repeat steps (7) and (8) for the sweeper frequencies listed in Table 4-16 for the 23 to 26.5 GHz band.

(25) Record the maximum response amplitude from Table 4-16.
(At frequency less than 18 GHz)

Maximum Response Amplitude (<18 GHz)_____dBc

(26) Record the maximum response amplitude from Table 4-16.
(At frequency ranging from 18 to 23 GHz)

Maximum Response Amplitude(<23 GHz) _____dBc

(27) Record the maximum response amplitude from Table 4-16.
(At frequency ranging from 23 to 26 GHz)

Maximum Response Amplitude(< 26.5GHz) _____dBc

The following steps are for the R3265.

[3.5 to 8 GHz Band (R3265 Only)]

(28) Set the R3265 center frequency to 7 GHz. Set the sweeper [CW] to 7 GHz.

(29) Rotate the CAL FACTOR switch to the power sensor's 7 GHz calibration factor on the power meter.

(30) On the sweeper, set the power level to the power meter indicate 0dBm.

On the R3265, press [PEAK] [MKR→] [MKR→CF] , [FREQ SPAN] [5] [MHz] ,
MARKER [ON] [NEXT MENU] [PRESELE] [PEAK SEARCH] [AUTO PEAKING] . Wait for the "peaking!!" message to disappear.

Press [MENU] [SWEEP MODE] [SINGLE SWP] , [PEAK] MARKER [ON] [MKR] [FIXED MKR ON/OFF] [FREQ SPAN]
[4] [0] [MHz] .

(31) Repeat steps (7) and (8) for the sweeper frequency listed in Table 4-17 for the 3.5 to 8GHz band's 7GHz center frequency.

(32) Set the R3265 center frequency to 8GHz. Set the sweeper [CW] to 8GHz.

(33) Rotate hte CAL FACTOR switch to the power sensor's 8GHz calibration factor on the power meter.

(34) Repeat step (30) for the R3265.

(35) Repeat steps (7) and (8) for the sweeper frequencies listed in Table 4-17 for the 3.5 to 8 GHz band's 8 GHz center frequency.

(36) Record the maximum response amplitude from Table 4-17.

Maximum Response Amplitude _____dBc

Table 4-16 Image, Multiple and Out-of-Band Responses (R3271)

Band	R3271 Center Freq. (GHz)	SG CW (MHz)	Response Amplitude (dBc)	Specification (dBc)
100 Hz to 3.6 GHz Band	2.0	1957.159		−70
	2.0	1157.159		−70
	2.0	10462.841		−70
	2.0	8231.4205		−70
3.5 GHz to 7.5 GHz Band	5.5	6342.841		−70
	5.5	11421.421		−70
	5.5	17342.841		−70
	5.5	23264.262		−50
7.4 GHz to 15.4 GHz Band	12.0	12842.841		−70
	12.0	5789.29		−70
	12.0	18210.71		−60
	12.0	24421.421		−50
15.2 GHz to 23.3 GHz Band	21.0	21842.841		−60
	21.0	6719.053		−70
	21.0	13859.527		−70
23 GHz to 26.5 GHz Band	24.4	25242.841		−60
	24.4	5783.935		−70
	24.4	11989.29		−70
	24.4	18194.645		−60

Table 4-17 Image, Multiple and Out-of-Band Responses (R3265)

Band	R3265 Center Freq. (GHz)	SG CW (MHz)	Response Amplitude (dBc)	Specification (dBc)
100 Hz to 3.6 GHz Band	2.0	1957.159		−70
	2.0	1157.159		−70
	2.0	10462.841		−70
	2.0	8231.4205		−70
3.5 GHz to 8 GHz Band	7.0	7842.841		−70
	8.0	4632.131		−70
	8.0	3789.29		−70

4.4.15 Frequency Response

- SPECIFICATION

R3265:
- ± 1.5 dB (100 Hz to 3.6 GHz) (10 dB Input Attenuation)
- ± 1.0 dB (50 MHz to 2.6 GHz)
- ± 1.5 dB (3.5 GHz to 7.5 GHz)
- ± 1.5 dB (7.4 GHz to 8 GHz)

R3271:
- ± 1.5 dB (100 Hz to 3.6 GHz)
- ± 1.0 dB (50 MHz to 2.6 GHz)
- ± 1.5 dB (3.5 GHz to 7.5 GHz)
- ± 3.5 dB (7.4 GHz to 15.4 GHz)
- ± 4.0 dB (15.4 GHz to 23.3 GHz)
- ± 4.0 dB (23 GHz to 26.5 GHz)

Frequency response relative to the calibrator (25 MHz): < ± 5 dB
Band switching uncertainty: < ± 0.5 dB

- RELATED ADJUSTMENT

  YTF adjustment.
  Frequency response adjustment.

- DESCRIPTION

  The sweeper signal is fed through a power splitter to a power sensor and the R3265/3271. The sweeper's power level is adjusted at 25 MHz to place the displayed signal at the R3265/3271 center horizontal graticule line. The power meter is placed in RATIO mode. At each new sweeper frequency, the sweeper's power level is adjusted to the center horizontal graticule line. The power meter displays the inverse of the frequency response relative to the calibrator.

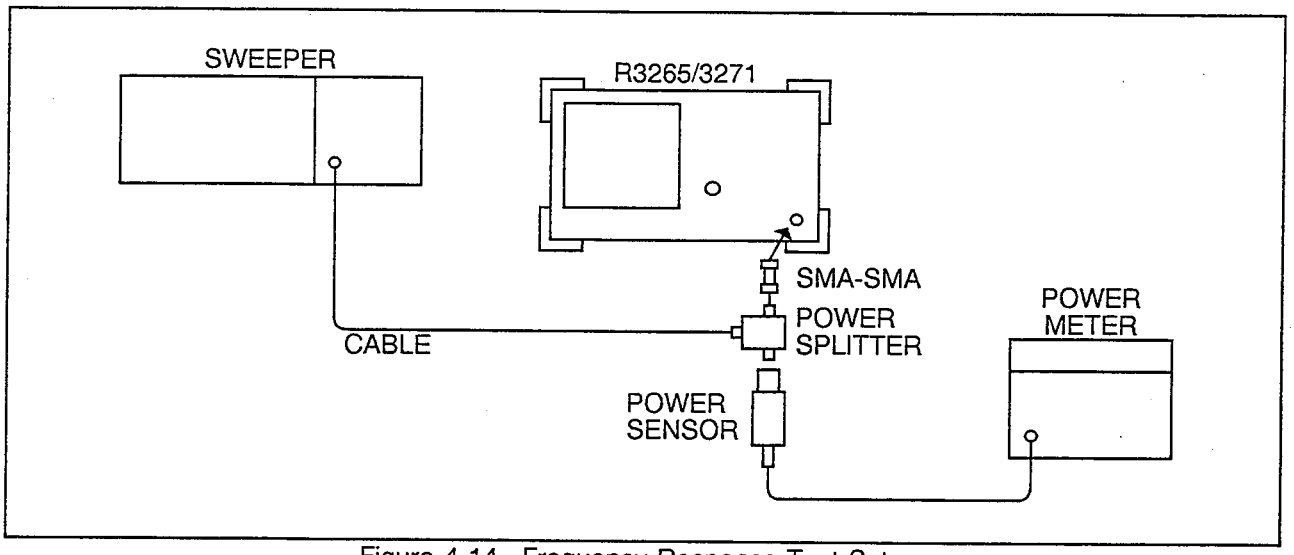


Figure 4-14 Frequency Response Test Setup

- EQUIPMENT

Sweeper	HP8350 + HP83595A
Power Meter	HP436A
Power Sensor	HP8485A
Power splitter	
Adapter:	
Type N to SMA	HRM-554S
SMA (m) to SMA (m)	50-673-0000-31
Cables:	
SMA, 70 cm	A01002

- PROCEDURE

(1) Zero and calibrate the power meter.

(2) Connect the equipment as shown in Figure 4-14.

(3) Press the [INSTR PRESET] key on the sweeper. Set the sweeper controls as follows:

CW	25 MHz
Freq Step	100 MHz
Power Level	−4 dBm

(4) On the R3265/3271, press the [PRESET] key.

Center Freq	25 MHz
CF Step	100 MHz
Span	40 MHz
Ref Level	– 5 dBm
dB/div	1 dB/div
RBW	3 MHz
VBW	1 KHz

(5) Press [PEAK] [NEXT MENU] [CONT PK ON/OFF].

(6) Adjust the sweeper [CW] vernier for a MKR frequency reading 100MHz ± 2MHz.

Adjust the sweeper POWER LEVEL for a MKR amplitude reading of – 10 dBm ± 0.09 dB.

(7) Press the [dB [REF]] switch on the power meter.

[Frequency Response (R3765/3271: 100 Hz to 3.6 GHz Band)]

(8) Set the sweeper [CW] to 100 MHz.

(9) Set the R3265/3271 [CENTER FREQ] to 100 MHz.

(10) Adjust the sweeper POWER LEVEL for an R3265/3271 MKR amplitude reading of – 10 dBm ± 0.09 dB.

(11) Record the reverse sign value of the power ratio displayed on the power meter in Table 4-18.

(12) On the sweeper, press the [CW] and [↑] keys.
On the R3265/3271, press the [CENTER FREQ] and [↑] keys.
At each new frequency, repeat steps (10) and (11), rotating the CAL FACTOR switch to the power sensor's calibration factor
Whne the peak is out of CRT display, adjust the [CW] VERNIER of the sweeper for near the center.

[Frequency Response (R3265/3271: 3.5 to 7.5 GHz Band)]

(13) Set the R3265/3271 [CENTER FREQ] to 3.6 GHz.

(14) Set the sweeper [CW] to 3.6 GHz.

(15) On the R3265/3271, press MARKER [ON] [NEXT MENU] [PRESELE] [PEAK SEARCH], [AUTO PEAKING].
Wait for the "peaking!!" message to disappear.

(16) Adjust the sweeper POWER LEVEL for an R3265/3271 MKR amplitude reading of −10 dBm ±0.09 dB.

(17) Record the reverse sign value of the power ratio displayed on the power meter in Table 4-19.

(18) On the sweeper, press the [CW] and [↑] keys.
On the R3265/3271, press the [CENTER FREQ] and [↑] keys.
At each new frequency, repeat steps (15) through (17), rotating the CAL FACTOR switch to the power sensor's calibration factor.
When the peak is out of CRT display, adjust the [CW] VERMER of sweeper for near the center.

[Frequency Response (R3265: 7.5 to 8.0 GHz Band) (R3271: 7.5 to 15.4 GHz Band)]

(19) Set the R3265/3271 [CENTER FREQ] to 7.5 GHz and [CF STEP AUTO/MNL] to 200 MHz.

(20) Set the sweeper [CW] to 7.5 GHz and [CW STEP SIZE] to 200 MHz.

(21) On the R3265/3271, press MARKER [ON] [NEXT MENU] [PRESELE] [PEAK SEARCH], [AUTO PEAKING].
Wait for the "peaking!!" message to disappear.

(22) Adjust the sweeper POWER LEVEL for an R3265/3271 MKR amplitude reading of −10 dBm ±0.09 dB.

(23) Recording the reverse sign value of the power ratio displayed on the power meter in Table 4-20.

(24) On the sweeper, press the [CW] and [↑] keys.
On the R3265/3271, press the [CENTER FREQ] and [↑] keys.
At each new frequency, repeat steps (21) through (23), rotating the CAL FACTOR switch to the power sensor's calibration factor.

[Frequency Response (R3271: 15.4 to 23.3 GHz Band)]

(25) Set the R3271 [CENTER FREQ] to 15.4 GHz.

(26) Set the sweeper [CW] to 15.4 GHz.

(27) On the R3271, press MARKER [ON] [NEXT MENU] [PRESELE] [PEAK SEARCH], [AUTO PEAKING].
Wait for the "peaking!!" message to disappear.

(28) Adjust the sweeper POWER LEVEL for an R3271 MKR amplitude reading of −10 dBm ±0.09 dB.

(29) Record the negative value of the power ratio displayed on the power meter in Table 4-21.

(30) On the sweeper, press the [CW] and [↑] keys.
On the R3271, press the [CENTER FREQ] and [↑] keys.
At each new frequency, repeat steps (27) through (29), rotating the CAL FACTOR switch to the power sensor's calibration factor.

[Frequency Response (R3271:233 to 26.5 GHz Band)]

(31) Set the R3271 [CENTER FREQ] to 23.4 GHz.

(32) Set the sweeper [CW] to 23.4 GHz.

(33) On the R3271, press MARKER [ON] [NEXT MENU] [PRESELE] [PEAK SEARCH], [AUTO PEAKING].
Wait for the "peaking!!" message to disappear.

(34) Adjust the sweeper POWER LEVEL for an R3271 MKR amplitude reading of −10 dBm ±0.09 dB.

(34) Adjust the sweeper POWER LEVEL for an R3271 MKR amplitude reading of −10 dBm ±0.09 dB.

(35) Record the reverse sign value of the power ratio displayed on the power meter in Table 4-22.

(36) On the sweeper, press the [CW] and [↑] keys.
On the R3271, press the [CENTER FREQ] and [↑] keys.
At each new frequency, repeat steps (33) through (35), rotating the CAL FACTOR switch to the power sensor's calibration factor.
When the peak is out of CRT display, adjust the [CW] VERNIER of the sweeper for near the center.

[Test Results]

(37) Frequency Response (R3265/3271:100 Hz to 3.6 GHz Band)

① Enter the most positive number from Table 4-18, HP436A Reading :_____dB
The absolute value of this number should be less than 5 dB.

② Enter the most negative number from Table 4-18, HP436A Reading:_____dB
The absolute value of this number should be less than 5 dB.

③ Subtract ② from ①: _____dB
The result should be less than 3 dB.

(38) Frequency Response (R3265/3271:50 MHz to 2.6 GHz Band)

① Enter most positive number from Table 4-18, HP436A Reading within the range of 100 MHz to 2.6 GHz frequency: _____dB

② Enter most negative number from Table 4-18, HP436A Reading within the range of 100 MHz to 2.6 GHz frequency: _____dB

③ Subtract ② from ①: _____dB
The result should be less than 2 dB.

(39) Frequency Response (R3265/3271:3.5 GHz to 7.5 GHz Band)

① Enter the most positive number from Table 4-19, HP436A Reading:_____dB
The absolute value of this number should be less than 5 dB.

② Enter the most negative number from Table 4-19, HP436A Reading:_____dB
The absolute value of this number should be less than 5 dB.

③ Subtract ② from ①: _____dB
The result should be less than 3 dB.

(40) Frequency Response (R3265:7.5 to 8 GHz Band)(R3271:7.5 to 15.4 GHz Band)

① Enter the most positive number from Table 4-20, HP436A Reading:_____dB
The absolute value of this number should be less than 5 dB.

② Enter the most negative number from Table 4-20, HP436A Reading:_____dB
The absolute value of this number should be less than 5 dB.

③ Subtract ② from ①: _____dB
The result should be less than 7 dB (R3265:3 dB).

(41) Frequency Response (R3271:15.4 to 23.3 GHz Band)

① Enter the most positive number from Table 4-21, HP436A Reading:_____dB
The absolute value of this number should be less than 5 dB.

② Enter the most negative number from Table 4-21, HP436A Reading:_____dB
The absolute value of this number should be less than 5 dB.

③ Subtract ② from ①: _____dB
The result should be less than 8 dB.

(42) Frequency Response (R3271:23.3 to 26.5 GHz Band)

① Enter the most positive number from Table 4-22, HP436A Reading:_____dB
The absolute value of this number should be less than 5 dB.

② Enter the most negative number from Table 4-22, HP436A Reading:_____dB
The absolute value of this number should be less than 5 dB.

③ Subtract ② from ①: _____dB
The result should be less than 8 dB.

Table 4-18 Frequency Response
(R3265/3271 : 100 Hz to 3.6 GHz Band)

Column 1	Column 2	Column 3
Frequency (MHz)	HP436A Reading (dB)	CAL Factor Freq. (GHz)
100		0.05
200		0.05
300		0.05
400		0.05
500		0.05
600		0.05
700		0.05
800		0.05
900		0.05
1000		0.05
1100		2.0
1200		2.0
1300		2.0
1400		2.0
1500		2.0
1600		2.0
1700		2.0
1800		2.0
1900		2.0
2000		2.0
2100		2.0
2200		2.0
2300		2.0
2400		2.0
2500		3.0
2600		3.0
2700		3.0
2800		3.0
2900		3.0
3000		3.0
3100		3.0
3200		3.0
3300		3.0
3400		3.0
3500		3.0

Table 4-19 Frequency Response
(R3265/3271 : 3.6 GHz to 7.5 GHz Band)

Column 1	Column 2	Column 3
Frequency (GHz)	HP436A Reading (dB)	CAL Factor Freq. (GHz)
3.6		4.0
3.7		4.0
3.8		4.0
3.9		4.0
4.0		4.0
4.1		4.0
4.2		4.0
4.3		4.0
4.4		4.0
4.5		5.0
4.6		5.0
4.7		5.0
4.8		5.0
4.9		5.0
5.0		5.0
5.1		5.0
5.2		5.0
5.3		5.0
5.4		5.0
5.5		6.0
5.6		6.0
5.7		6.0
5.8		6.0
5.9		6.0
6.0		6.0
6.1		6.0
6.2		6.0
6.3		6.0
6.4		6.0
6.5		7.0
6.6		7.0
6.7		7.0
6.8		7.0
6.9		7.0
7.0		7.0
7.1		7.0
7.2		7.0
7.3		7.0
7.4		7.0

Table 4-20 Frequency Response
(R3265 : 7.5 GHz to 8 GHz Band)
(R3271 : 7.5 GHz to 15.4 GHz Band)

Column 1	Column 2	Column 3
Frequency (GHz)	HP436A Reading (dB)	CAL Factor Freq. (GHz)
7.5		8.0
7.7		8.0
7.9		8.0
<R3271 Only>		
8.1		8.0
8.3		8.0
8.5		9.0
8.7		9.0
8.9		9.0
9.1		9.0
9.3		9.0
9.5		10.0
9.7		10.0
9.9		10.0
10.1		10.0
10.3		10.0
10.5		11.0
10.7		11.0
10.9		11.0
11.1		11.0
11.3		11.0
11.5		12.0
11.7		12.0
11.9		12.0
12.1		12.0
12.3		12.0
12.5		13.0
12.7		13.0
12.9		13.0
13.1		13.0
13.3		13.0
13.5		14.0
13.7		14.0
13.9		14.0
14.1		14.0
14.3		14.0
14.5		15.0
14.7		15.0
14.9		15.0
15.1		15.0
15.3		15.0

Table 4-21 Frequency Response
(R3271 : 15.4 GHz to 23.3 GHz Band)

Column 1	Column 2	Column 3
Frequency (GHz)	HP436A Reading (dB)	CAL Factor Freq. (GHz)
15.4		15.0
15.6		16.0
15.8		16.0
16.0		16.0
16.2		16.0
16.4		16.0
16.6		17.0
16.8		17.0
17.0		17.0
17.2		17.0
17.4		17.0
17.6		18.0
17.8		18.0
18.0		18.0
18.2		18.0
18.4		18.0
18.6		19.0
18.8		19.0
19.0		19.0
19.2		19.0
19.4		19.0
19.6		20.0
19.8		20.0
20.0		20.0
20.2		20.0
20.4		20.0
20.6		21.0
20.8		21.0
21.0		21.0
21.2		21.0
21.4		21.0
21.6		22.0
21.8		22.0
22.0		22.0
22.2		22.0
22.4		22.0
22.6		23.0
22.8		23.0
23.0		23.0
23.2		23.0

Table 4-22 Frequency Response
(R3271 : 23.3 GHz to 26.5 GHz Band)

Column 1	Column 2	Column 3
Frequency (GHz)	HP436A Reading (dB)	CAL Factor Freq. (GHz)
23.4		23.0
23.6		24.0
23.8		24.0
24.0		24.0
24.2		24.0
24.4		24.0
24.6		25.0
24.8		25.0
25.0		25.0
25.2		25.0
25.4		25.0
25.6		26.0
25.8		26.0
26.0		26.0
26.2		26.0
26.4		26.0

4.4.16 IF Gain Uncertainty

- SPECIFICATION

  IF Gain Uncertainty:
  < ±0.5 dB, reference levels 0 dBm to −50 dBm with 10 dB input attenuation
  < ±0.7 dB, reference levels 0 dBm to −80 dBm with 10 dB input attenuation

- RELATED ADJUSTMENT
  IF amplitude adjustment.

- DESCRIPTION
  This test measures IF gain error in resolution band width 1 MHz, 3 kHz and 300 kHz. The input signal level is decreased as the spectrum analyzer's reference level is decreased (IF gain increased). Since the signal level is decreased in precise steps, any error between the reference level and the signal level is caused by the analyzer's IF gain. The frequency synthesizer is phase-looked to the analyzer's 10 MHz reference.

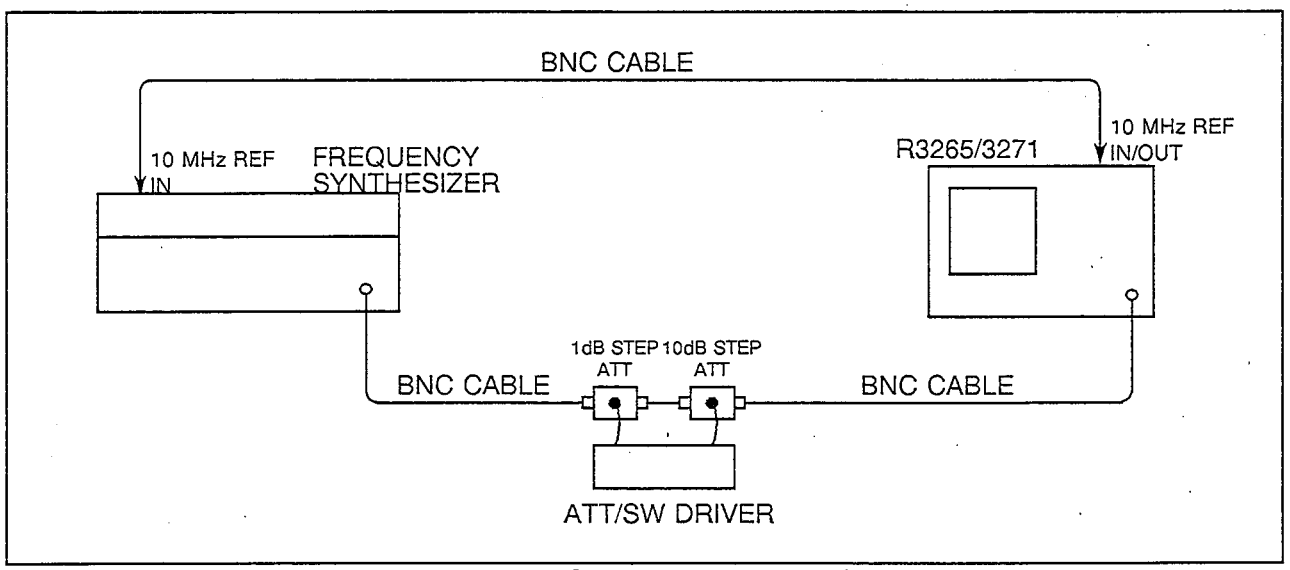


Figure 4-15 IF Gain Uncertainty Test Setup

- EQUIPMENT

Frequency Synthesizer	HP3325B
1 dB Step Attenuator	HP8494H
10 dB Step Attenuator	HP8495H
Attenuator/Switch Driver	HP11713A

- PROCEDURE

(1) Connect the equipment as shown in Figure 4-15.

(2) Set the frequency synthesizer controls as follows:

Freq	11 MHz
Amplitude	−5 dBm

(3) On the R3265/3271, press the [PRESET] key and set the controls as follows:

Center Freq	11 MHz
Freq Span	0 Hz
dB/div	1 dB
VBW	1 Hz
RBW	1 MHz

(4) Set 1 dB and 10 dB step attenuator to 0 dB. Set the output level of the frequency synthesizer to the value 5 dB lower than the R3265/3271 reference level.

(5) After several sweeps in the R3265/3271, press the [A] [VIEW A] and [PEAK] keys to read the data on the screen and record it as the reference value. Then, press the [ON], [MKR], [B] keys and [WRITE B].

(6) Press the 1 dB step attenuator to lower the R3265/3271 reference level by 1 dB.

(7) After several sweeps in the R3265/3271, press the [PEAK] key to read the marker level on the screen and record it in Table 4-23.

(8) Repeat steps (6) and (7) until the 1 dB step attenuator is lowered to 10 dB.

(9) Press the 10 dB step attenuator to lower the R3265/3271 reference level by 10 dB.

(10) After several sweeps in the R3265/3271, press the [PEAK] key to read the data on the screen and record it in Table 4-23.

(11) Repeat steps (9) and (10) until the 10 dB attenuator is lowered to 60 dB.

(12) Repeat steps (2) to (11) above for the R3265/3271 resolution band width 3 kHz and 300 kHz. For resolution band width 3 kHz, repeat steps (11) until the 10 dB step attenuator is lowered to 70 dB and record the result in Table 4-24. For resolution band width 300 kHz, set dB/div to 0.5 dB/div in step (3) and record the result in Table 4-25.

Table 4-23 IF Gain Error (RBW = 1 MHZ, 1 dB/div.)

Reference value (dBm)

R3265/3271 Reference Level (dBm)	1 dB Step Attenuator Attenuation (dB)	10 dB Step Attenuator Attenuation (dB)	⊿ Marker Level (dB)	Specification
0	0	0	0 (Ref.)	–
−1	1	0		±0.5 dB
−2	2	0		±0.5 dB
−3	3	0		±0.5 dB
−4	4	0		±0.5 dB
−5	5	0		±0.5 dB
−6	6	0		±0.5 dB
−7	7	0		±0.5 dB
−8	8	0		±0.5 dB
−9	9	0		±0.5 dB
−10	10	0		±0.5 dB
−20	10	10		±0.5 dB
−30	10	20		±0.5 dB
−40	10	30		±0.5 dB
−50	10	40		±0.5 dB
−60	10	50		±0.7 dB
−70	10	60		±0.7 dB

Table 4-24 IF Gain Error (RBW = 3 kHZ, 1 dB/div.)

Reference value (dBm)

R3265/3271 Reference Level (dBm)	1 dB Step Attenuator Attenuation (dB)	10 dB Step Attenuator Attenuation (dB)	⊿ Marker Level (dB)	Specification
0	0	0	0 (Ref.)	–
−1	1	0		±0.5 dB
−2	2	0		±0.5 dB
−3	3	0		±0.5 dB
−4	4	0		±0.5 dB
−5	5	0		±0.5 dB
−6	6	0		±0.5 dB
−7	7	0		±0.5 dB
−8	8	0		±0.5 dB
−9	9	0		±0.5 dB
−10	10	0		±0.5 dB
−20	10	10		±0.5 dB
−30	10	20		±0.5 dB
−40	10	30		±0.5 dB
−50	10	40		±0.5 dB
−60	10	50		±0.7 dB
−70	10	60		±0.7 dB
−80	10	70		±0.7 dB

Table 4-25 IF Gain Error (RBW = 300 kHZ, 0.5 dB/div.)

Reference value (dBm)

R3265/3271 Reference Level (dBm)	1 dB Step Attenuator Attenuation (dB)	10 dB Step Attenuator Attenuation (dB)	⊿ Marker Level (dB)	Specification
0	0	0	0 (Ref.)	–
−1	1	0		±0.5 dB
−2	2	0		±0.5 dB
−3	3	0		±0.5 dB
−4	4	0		±0.5 dB
−5	5	0		±0.5 dB
−6	6	0		±0.5 dB
−7	7	0		±0.5 dB
−8	8	0		±0.5 dB
−9	9	0		±0.5 dB
−10	10	0		±0.5 dB
−20	10	10		±0.5 dB
−30	10	20		±0.5 dB
−40	10	30		±0.5 dB
−50	10	40		±0.5 dB
−60	10	50		±0.7 dB
−70	10	60		±0.7 dB

4.4.17 Scale Fidelity

- SPECIFICATION

  Log Scale Fidelity: ± 0.2 dB/1 dB,
  ± 1 dB/10 dB to a maximum of ± 1.5 dB over 0 to 90 dB range.
  Linear Scale Fidelity: < ± 5% of reference level
  QP-mode Log Scale Fidelity: ± 1.0 dB/30 dB, ± 2dB/40 dB, ± 1.0 dB/40 dB (25°C ± 10°C)

- RELATED ADJUSTMENT
  IF amplitude adjustment.

- DESCRIPTION
  This test measures display accuracy for 1 dB, 10 dB log scales, X1, X2 linear scales and 10 dB QP mode log scale. All scales are measured with 0 dBm reference signal. Figure 4-16 illustrates the measurement system of this test. The frequency synthesizer is phase-locked to the 10 MHz reference source of the spectrum analyzer.

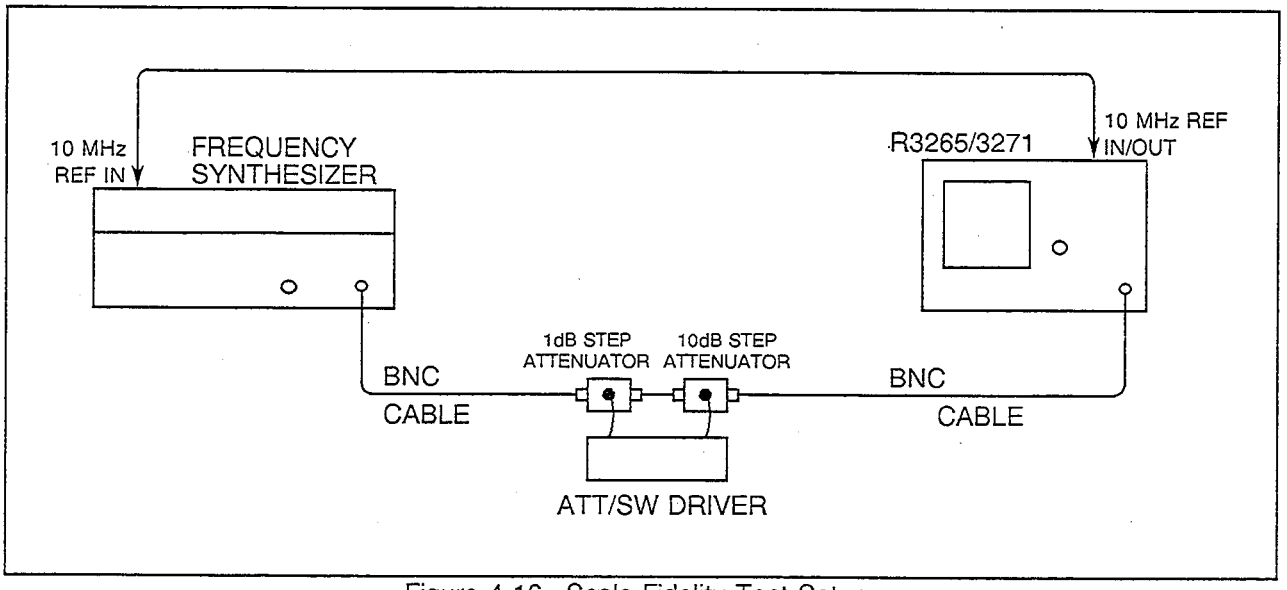


Figure 4-16 Scale Fidelity Test Setup

- EQUIPMENT

Frequency Synthesizer	HP3325B
1 dB Step Attenuator	HP8494H
10 dB Step Attenuator	HP8495H
Attenuator/Switch Driver	HP11713A

- PROCEDURE

(1) Connect the equipment as shown in Figure 4-16.

(2) Set the frequency synthesizer controls as follows:

Freq	11 MHz
Amplitude	0 dBm

(3) On the R3265/3271, press the [PRESET] key and set the controls as follows:

Center Freq	11 MHz
Freq Span	0 Hz
Ref Level	0 dBm
RBW	1 MHz
VBW	1 Hz
dB/div	1 dB/div

(4) Set the 1 dB and 10 dB step attenuators to 0 dB.

(5) On the R3265/3271, press the MARKER [ON] key.

[1 dB/div Log Scale]

(6) On the frequency synthesizer, adjust the amplitude until the R3265/3271 marker reads exactly 0.00 dBm.

(7) On the R3265/3271, press the [A], [VIEW A], MARKER [ON] and [⊿ MKR] keys. Then press the [B] and [WRITE B].

(8) On the R3265/3271, press the [MENU] key, [SWEEP MODE], [SINGLE SWP].

(9) Lower the frequency synthesizer level by 1 dB.

(10) On the R3265/3271, press the [MENU] key, [SWEEP MODE], [SINGLE SWP] and [SINGLE SWP].

(11) Record the ⊿ marker level in the Actual Columm in Table 4-26. Calculate the incremental error according to the following equation and record the result in the Incremental Error column in Table 4-26.
Incremental error = (Current ⊿ marker level) - (Previous ⊿ marker level) + 1 dB

(12) Repeat steps (9) to (11) until the frequency synthesizer level is set to the value 10 dB lower than the initially set level.

[10 dB/div Log Scale]

(13) On the R3265/3271, press the [MENU] [SWEEP MODE] and [CONT SWP] keys set [REF LEVEL] and [dB/div] to 10 dB/div. Set the resolution band width to 3 kHz.

(14) Set the frequency synthesizer level so that the R3265/3271 marker indicates just 0.00 dBm.

(15) On the R3265/3271, press the [A], [VIEW A] MARKER [ON] and [⊿ MKR] keys. Then press the [B] and [WRITE B].

(16) Lower the frequency synthesizer level by 10 dB. If the level cannot be lowered by 10 dB, use the 10 dB step attenuator to lower it by 10 dB.

(17) On the R3265/3271, press the [MENU], [SWEEP MODE], [SINGLE SWP] and [SINGLE SWP] keys.

(18) Record the ⊿marker level in the Actual columm in Table 4-27. Calculate the incremental error from the following expression and record the result in the Incremental Error column in Table 4-27.
Incremental error = (Current ⊿ marker level) - (Previous ⊿ marker level) + 10 dB

(19) Repeat steps (16) to (18) until the frequency synthesizer level is set to the value 90 dB lower than the initially set level.

Table 4-26 1 dB/div. Log Scale Fidelity (RBW = 1 MHz)

Input Signal Level (dBm, nominal)	dB from Reference Level (nominal)	⊿ Marker Level			Incremental Error (dB)
		Min. (dBm)	Actual (dBm)	Max. (dBm)	
0	0	0	0 (Ref.)	0	0 (Ref.)
−1	−1	−1.2		−0.8	
−2	−2	−2.4		−1.6	
−3	−3	−3.6		−2.4	
−4	−4	−4.8		−3.2	
−5	−5	−6.0		−4.0	
−6	−6	−7.0		−5.0	
−7	−7	−8.0		−6.0	
−8	−8	−9.0		−7.0	
−9	−9	−10.0		−8.0	
−10	−10	−11.0		−9.0	

Table 4-27 10 dB/div. Log Scale Fidelity (RBW = 3 kHz)

Input Signal Level (dBm, nominal)	dB from Reference Level (nominal)	⊿ Marker Level			Incremental Error (dB)
		Min. (dBm)	Actual (dBm)	Max. (dBm)	
0	0	0	0 (Ref.)	0	0 (Ref.)
−10	−10	−11		−9	
−20	−20	−21.5		−18.5	
−30	−30	−31.5		−28.5	
−40	−40	−41.5		−38.5	
−50	−50	−51.5		−48.5	
−60	−60	−61.5		−58.5	
−70	−70	−71.5		−68.5	
−80	−80	−81.5		−78.5	
−90	−90	−91.5		−88.5	

[Linear Scale]

(20) Set the frequency synthesizer as follows:

Freq	11 MHz
Amplitude	0 dBm

Set the 1 dB and 10 dB attenuator to 0 dB.

(21) On the R3265/3271, press the [PRESET] key and set the controls as follows:

Center Freq	11 MHz
Freq Span	10 kHz
Ref Level	0 dBm
RBW	1 kHz
VBW	1 kHz
ATT	20 dB

(22) On the R3265/3271, press the [REF LEVEL], [LINEAR] and [X1] keys to select the linear X1 mode. Then, press the MARKER [ON] key.

(23) Precisely set the frequency synthesizer level to the R3265/3271 reference level while reading the marker level on the screen.

(24) On the R3265/3271, press the [MENU], [SWEEP MODE] and [SINGLE SWP] keys to set the single sweep mode.

(25) Read the level value displayed on the frequency synthesizer and set the value as the reference value (Ref). Then, set the frequency synthesizer level to the value 0.92 dB lower than the reference value.

(26) On the R3265/3271, perform single sweep twice, read the marker level and record it in Table 4-28.

(27) Set the frequency synthesizer level as shown in the Input Signal Level column in Table 4-28 sequentially and repeat step (26) for each.

Table 4-28 Linear Scale Fidelity (X1)

Input Signal Level		Div. from Reference Level	Marker Level		
(dB, nominal)	(mV, nominal)		Min. (mV)	Actual (mV)	Max. (mV)
0 (Ref.)	223.6	0	223.6	223.6 (Ref.)	223.6
−0.92	201.24	1	190.06		212.42
−1.94	178.88	2	167.7		190.06
−3.10	156.52	3	145.34		167.7
−4.44	134.16	4	122.98		145.34
−6.02	111.8	5	100.62		122.98
−7.96	89.44	6	78.26		100.62
−10.46	67.08	7	55.9		78.26
−13.98	44.72	8	33.54		55.9
−20	22.36	9	11.18		33.54

Table 4-29 QP-mode Log Scale Fidelity

Input Signal Level (dBm, nominal)	dB from Reference Level (dB, nominal)	⊿ Marker Level		
		Min. (dBm)	Actual (dBm)	Max. (dBm)
0 (Ref.)	0	0	0 (Ref.)	0
−10	−10	−11		−9
−20	−20	−21		−19
−30	−30	−31		−29
−40	−40	−41*		−39**

*: −42 dBm when the ambient temperature is out of range 25°C ±10°C.
**: −38 dBm whe the ambient temperature is out of range 25°C ±10°C.

[QP-mode Log Scale]

(28) Set the frequency synthesizer as follows:

Freq	11 MHz
Amplitude	0 dBm

Set the 1dB and 10dB attenuator to 0dB.

(29) On the R3265/3271, press the [PRESET] key and set the controls as follows:

Center Freq	11 MHz
Freq Span	0 Hz

(30) On the R3265/3271, press the [SHIFT] , [EMC 1] [QP] keys to set the QP mode.

Then, press the MARKER [ON] key.

(31) Precisely set the frequency synthesizer level to the R3265/3271 reference level.

(32) On the R3265/3271, press the [A] , [VIEW A] MARKER [ON] and [⊿ MKR] keys.

Then, press the [B] key and [WRITE B] .

(33) Lower the frequency synthesizer level by 10 dB. After (2) to (3) seconds, read the ⊿ marker level on the screen and record it in Table 4-29.

(34) Repeat step (33) until the frequency synthesizer level is set to the value 40 dB lower than the level set in step (31).

4.4.18 Input Attenuator Accuracy

- SPECIFICATION

Input attenuator accuracy (referenced to 10 dB input attenuation, for 20 to 70 dB settings):

R3265: 100 Hz to 8 GHz: < ±1.1 dB/10 dB step to a maximum of ±2.0 dB

R3271:
- 100 Hz to 12.4 GHz: < ±1.1 dB/10 dB step to a maximum of ±2.0 dB
- 12.4 GHz to 18 GHz: < ±1.3 dB/10 dB step to a maximum of ±2.5 dB
- 18 GHz to 26.5 GHz: < ±1.8 dB/10 dB step to a maximum of ±3.5 dB

- RELATED ADJUSTMENT

There is no related adjustment procedure for this performance test.

- DESCRIPTION

This test measures the input attenuator's switching accuracy over the full 70 dB.
The number of frequency measured points is one point at 4 GHz for the R3265, and three points at 4 GHz, 15 GHz and 18 GHz for the R3271.
The synthesized sweeper is phase-locked to the spectrum analyzer's 10 MHz reference. The input attenuator switching accuracy is referenced to the 10 dB attenuator setting. Step-to-step accuracy is calculated from switching accuracy data.

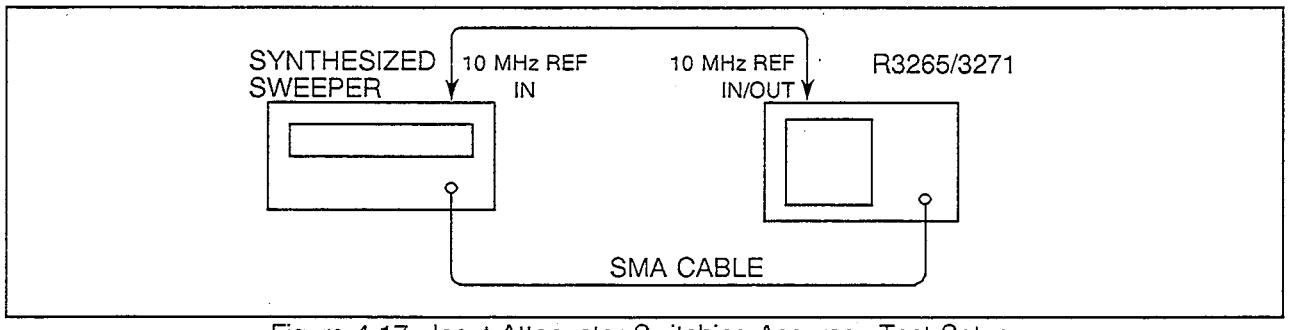


Figure 4-17 Input Attenuator Switching Accuracy Test Setup

- EQUIPMENT

Synthesized Sweeper :

Frequency Range:10 MHz to 18 GHz	TR4515
(Critical Specifications for Equipment Substitution)	(Recommended model)

- PROCEDURE

(1) IF gain uncertainty is measured when the resolution bandwidth is set to 3kHz and the result is filled in on the IF Gain uncertainty of Table 4-30.
For the test method, refer to "4.4.16 IF Gain Uncertainty".

CAUTION

Measure IF gain uncertainty when the resolution bandwidth is set to 3kHz before doing this test.
IF gain uncertainty is included in the measurement result because of IF gain's changing and measuring in this test.

(2) Connect the equipment as shown in Figure 4-17.

(3) Set the synthesized generator controls as follows:

Freq	4 GHz
Amplitude	-5 dBm

(4) On the R3265/3271, press the [PRESET] key and set the controls as follows:

Center Freq	4 GHz
Freq Span	10 kHz
Ref Level	0 dBm
dB/div	1 dB/div
RBW	3 kHz
VBW	10 Hz
SWP	1 sec

(5) On the synthesized generator, adjust the POWER LEVEL to place the peak of the signal five divisions below the R3265/3271 reference level.

(6) On the R3265/3271, press the [MENU] key, [SWEEP MODE], [SINGLE SWP] and [SINGLE SWP].

Press the [PEAK] key, read the MKR level and record it in Table 4-30 as the reference value.

(7) On the R3265/3271, press the [CPL], [ATT] and [↑] keys.

(8) On the R3265/3271, press the [MENU] key, [SWEEP MODE] [SINGLE SWP] and [SINGLE SWP].

Press the [PEAK] key, read the MKR level. The marker level measured here is subtracted from the reference value measure in the (6).
IF gain uncertainty measured in the (1) is subtracted from the value.

Records it in Table 4-30 as Actual MKR Reading.

Actual MKR Reading	=	Reference value measured in the (6)	-	Marker level measured in the (9)	-	IF gain uncertainty measured in the (1)

(9) Repeat steps (7) and (8) for the remaining R3265/3271 ATT setting listed in Table 4-30.

(10) Calculate the step-to-step accuracy as described in the following steps and record the results in Table 4-30. Step-to-step accuracy should be within the limits shown in Table 4-30.

[Step-to-Step Accuracy Calculation]

(11) For the 20 dB ATT setting, switching accuracy becomes step-to-step accuracy.

(12) For the 30, 40, 50, 60 and 70 dB ATT settings, subtract the 10dB down ATT switching accuracy from the current ATT switching accuracy.

(13) Center Frequency is changed to 15GHz and 18GHz and the operations in (2) to (12) are executed for R3271. Fill in the value measured in the (1) when Center Frequency is 4GHz on the IF Gain Uncertainty Table 4-30.

Table 4-30 Input Attenuator Accuracy

[R3265] Center Frequency: 4 GHz, Reference value____dBm

R3265 Attenuator (dB)	IF Gain (dB)	IF Gain Uncertainty (dB)	Switching Accuracy			Step-to-Step Accuracy	
			Min. (dB)	Actual (dB)	Max. (dB)	Actual (dB)	Spec. (dB)
10	0	0	0 (Ref.)	0 (Ref.)	0 (Ref.)	0 (Ref.)	0 (Ref.)
20	10		-2		+2		±1.1
30	20		-2		+2		±1.1
40	30		-2		+2		±1.1
50	40		-2		+2		±1.1
60	50		-2		+2		±1.1
70	60		-2		+2		±1.1

[R3271] Center Frequency: 4 GHz, Reference value____dBm

R3271 Attenuator (dB)	IF Gain (dB)	IF Gain Uncertainty (dB)	Switching Accuracy			Step-to-Step Accuracy	
			Min. (dB)	Actual (dB)	Max. (dB)	Actual (dB)	Spec. (dB)
10	0	0	0 (Ref.)	0 (Ref.)	0 (Ref.)	0 (Ref.)	0 (Ref.)
20	10		-2		+2		±1.1
30	20		-2		+2		±1.1
40	30		-2		+2		±1.1
50	40		-2		+2		±1.1
60	50		-2		+2		±1.1
70	60		-2		+2		±1.1

[R3271] Center Frequency: 15 GHz, Reference value____dBm

R3271 Attenuator (dB)	IF Gain (dB)	IF Gain Uncertainty (dB)	Switching Accuracy			Step-to-Step Accuracy	
			Min. (dB)	Actual (dB)	Max. (dB)	Actual (dB)	Spec. (dB)
10	0	0	0 (Ref.)	0 (Ref.)	0 (Ref.)	0 (Ref.)	0 (Ref.)
20	10		-2.5		+2.5		±1.3
30	20		-2.5		+2.5		±1.3
40	30		-2.5		+2.5		±1.3
50	40		-2.5		+2.5		±1.3
60	50		-2.5		+2.5		±1.3
70	60		-2.5		+2.5		±1.3

[R3271] Center Frequency: 15 GHz, Reference value____dBm

R3271 Attenuator (dB)	IF Gain (dB)	IF Gain Uncertainty (dB)	Switching Accuracy			Step-to-Step Accuracy	
			Min. (dB)	Actual (dB)	Max. (dB)	Actual (dB)	Spec. (dB)
10	0	0	0 (Ref.)	0 (Ref.)	0 (Ref.)	0 (Ref.)	0 (Ref.)
20	10		-3.5		+3.5		±1.8
30	20		-3.5		+3.5		±1.8
40	30		-3.5		+3.5		±1.8
50	40		-3.5		+3.5		±1.8
60	50		-3.5		+3.5		±1.8
70	60		-3.5		+3.5		±1.8

4.4.19 Sweep Time Accuracy

- SPECIFICATION

  For Span = 0 Hz
  Sweep Time ≤ ±3%

- RELATED ADJUSTMENT
  There is no related adjustment procedure for this performance test.

- DESCRIPTION
  A low frequency signal (Square Wave) is displayed on the R3265/3271 Spectrum Analyzer in ZERO Span mode, and measure the frequency of the displayed signal.

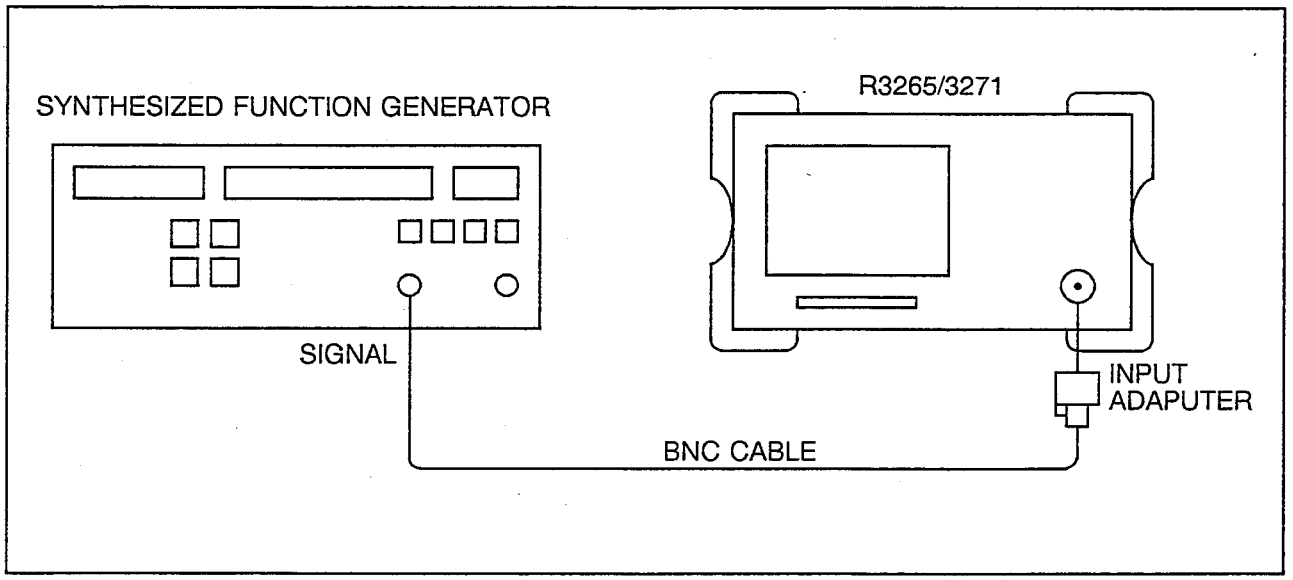


Figure 4-18 Sweep Time Accuracy Test Setup

- EQUIPMENT

  Synthesized Function Generator HP3325A

Adapters:
  Type N(m)to-BNC(f) JCF-AF00IEXO3

Cable:
  BNC, 150 cm MI-09

- PROCEDURE

(1) Connect the equipment as shown in Figure 4-18 using the BNC cable from the HP3325A SIGNAL OUT.
Connected it to the R3265/3271 INPUT.

(2) On the R3265/3271, press the [PRESET] key and set the controls as follows:

Center Freq	0 MHz
Span	0 MHz
Sweep Time	50 µs
dB/div	1 dB/div

(3) On the HP3325A, set the controls as follows:

Frequency	22 kHz
Amplitude	−10 dBm
Function	Square

(4) On the R3265/3271, press [MENU] key, set [TRIG] and [VIDEO], and adjust with the knob to trigger with VIDEO. And press the [MENU] key, [SWEEP MODE], [SINGLE] and [SINGLE].
Wait for the sweeper stops.

(5) On the R3265/3271, press the MARKER [ON] key. Set the marker at the second rising edge from left.
Record the Marker time as the Measured Sweep Time in Table 4-31 for the 50 s Sweep Time setting.
The Measured Sweep Time should be within the limits shown in Table 4-31.

(6) Repeat step (5) for the HP3325A frequencies and R3265/3271 sweep times as indicated in Table 4-31.

Table 4-31 Sweep Time Accuracy

HP3325A Frequency	R3265/3271 Sweep Time Setting	Marker Reading		
		Min.	Actual	Max.
22 kHz	50 µs	44.1 µs		46.8 µs
11 kHz	100 µs	88.2 µs		93.6 µs
5.5 kHz	200 µs	177 µs		187 µs
2.2 kHz	500 µs	441 µs		468 µs
1.1 kHz	1 ms	882 µs		936 µs
550 Hz	2 ms	1.77 ms		1.87 ms
220 Hz	5 ms	4.41 ms		4.68 ms
110 Hz	10 ms	8.82 ms		9.36 ms
55 Hz	20 ms	17.7 ms		18.7 ms
22 Hz	50 ms	44.1 ms		46.8 ms
11 Hz	100 ms	88.2 ms		93.6 ms
5.5 Hz	200 ms	177 ms		187 ms
2.2 Hz	500 ms	441 ms		468 ms
1.1 Hz	1 s	882 ms		936 ms
0.55 Hz	2 s	1.77 s		1.87 s
0.22 Hz	5 s	4.41 s		4.68 s
0.11 Hz	10 s	8.82 s		9.36 s
0.055 Hz	20 s	17.7 s		18.7 s
0.022 Hz	50 s	44.1 s		46.8 s
0.011 Hz	100 s	88.2 s		93.6 s

4.4.20 Calibration Amplitude Accuracy

- SPECIFICATION

  Amplitude: – 10 dBm ± 0.3 dB

- RELATED ADJUSTMENT
  Calibration amplitude adjustment.

- DESCRIPTION
  The amplitude accuracy of the CALOUT signal are checked for – 10 dBm ± 0.3 dBm.

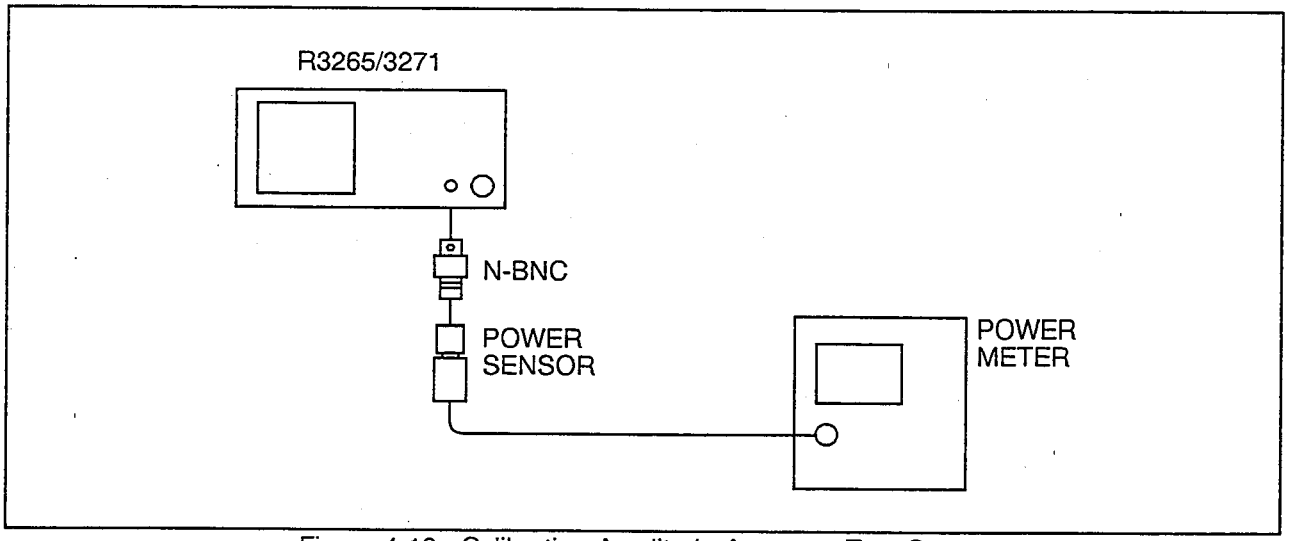


Figure 4-19 Calibration Amplitude Accuracy Test Setup

- EQUIPMENT

  Power Meter HP436A
  Power Sensor HP8481A

- PROCEDURE

  (1) Connect the equipment as shown in Figure 4-19.

  (2) Press the power sensor zero of the power meter and calibrate the power sensor. Enter the power sensor's 25 MHz calibration factor into the power meter.

  (3) Connect the power sensor via an N(f) – BNC(m) adapter directly to the CALOUT connector. Read the power meter display. The power level should be within the following limits (± 0.3 dB):

  Actual
  – 10.3 dBm ≤ _____ ≤ – 9.7 dBm

4.5 Checklist/Data Form

File No. :_____ Description : SPECTRUM ANALYZER

UUT MFR : ADVANTEST CO. ID No. :_____

Model : R3265/3271 Date :_____

Table 4-32 Performance Test Record (1 of 12)

Para. No.	Test Description	Results		
		Min.	Actual	Max.
1	Frequency Readout Accuracy and Frequency Counter Marker Accuracy			
	2.0 GHz CENTER FREQ			
	1 MHz SPAN	1.99994829 GHz		2.00005171 GHz
	10 MHz SPAN	1.99968479 GHz		2.00031521 GHz
	20 MHz SPAN	1.99935479 GHz		2.00064521 GHz
	50 MHz SPAN	1.99845479 GHz		2.00154521 GHz
	100 MHz SPAN	1.99684979 GHz		2.00315021 GHz
	2 GHz SPAN	1.93954979 GHz		2.06045021 GHz
	5.0 GHz CENTER FREQ			
	1 MHz SPAN	4.99994799 GHz		5.00005201 GHz
	10 MHz SPAN	4.99968449 GHz		5.00031551 GHz
	20 MHz SPAN	4.99935449 GHz		5.00064551 GHz
	50 MHz SPAN	4.99845449 GHz		5.00154551 GHz
	100 MHz SPAN	4.99684949 GHz		5.00315051 GHz
	2 GHz SPAN	4.93954949 GHz		5.06045051 GHz
	<R3271 ONLY>			
	11.0 GHz CENTER FREQ			
	1 MHz SPAN	10.99994739 GHz		11.00005261 GHz
	10 MHz SPAN	10.99968389 GHz		11.00031611 GHz
	20 MHz SPAN	10.99935389 GHz		11.00064611 GHz
	50 MHz SPAN	10.99845389 GHz		11.00154611 GHz
	100 MHz SPAN	10.99684889 GHz		11.00315111 GHz
	2 GHz SPAN	10.93954889 GHz		11.06045111 GHz
	18.0 GHz CENTER FREQ			
	1 MHz SPAN	17.99994669 GHz		18.00005331 GHz
	10 MHz SPAN	17.99968319 GHz		18.00031681 GHz
	20 MHz SPAN	17.99935319 GHz		18.00064681 GHz
	50 MHz SPAN	17.99845319 GHz		18.00154681 GHz
	100 MHz SPAN	17.99684819 GHz		18.00315181 GHz
	2 GHz SPAN	17.93954819 GHz		18.06045181 GHz

Table 4-32 Performance Test Record (2 of 12)

Para. No.	Test Description	Results		
		Min.	Actual	Max.
1	Frequency Readout Accuracy and Frequency Counter Marker Accuracy (cont'd)			
	Frequency Counter Marker Accuracy			
	2.0 GHz CENTER FREQ	1.999999794 GHz		2.000000206 GHz
	5.0 GHz CENTER FREQ	4.999999494 GHz		5.000000506 GHz
	11.0 GHz CENTER FREQ	10.999998889 GHz		11.000001111 GHz
	18.0 GHz CENTER FREQ	17.999998184 GHz		18.000001816 GHz
2	Frequency Reference Output Accuracy			
	10 MHz Reference Frequency	24.9999975 MHz		25.0000025 MHz
3	Residual FM			
	Residual FM			3 Hz
4	Frequency Drift			
	50.1 kHz SPAN			2.5 kHz
	200 Hz SPAN			60 Hz
5	Noise Sidebands			
	2.6 GHz Center Frequency			
	1 kHz Offset			−100 dBc/Hz
	10 kHz Offset			−110 dBc/Hz
	100 kHz Offset			−114 dBc/Hz
	3.7 GHz Center Frequency			
	1 kHz Offset			−95 dBc/Hz
	10 kHz Offset			−108 dBc/Hz
	100 kHz Offset			−110 dBc/Hz

Table 4-32 Performance Test Record (3 of 12)

Para. No.	Test Description	Results		
		Min.	Actual	Max.
6	Frequency Span Accuracy			
	2 GHz Center Frequency			
	20 kHz SPAN	15.2 kHz		16.8 kHz
	50 kHz SPAN	38.0 kHz		42 kHz
	400 kHz SPAN	304 kHz		336 kHz
	2 MHz SPAN	1.52 MHz		1.68 MHz
	2.01 MHz SPAN	1.552 MHz		1.648 MHz
	5 MHz SPAN	3.88 MHz		4.12 MHz
	10 MHz SPAN	7.76 MHz		8.24 MHz
	20 MHz SPAN	15.52 MHz		16.48 MHz
	50 MHz SPAN	38.8 MHz		41.2 MHz
	100 MHz SPAN	77.6 MHz		82.4 MHz
	200 MHz SPAN	155.2 MHz		164.8 MHz
	500 MHz SPAN	388 MHz		412 MHz
	1 GHz SPAN	776 MHz		824 MHz
	2 GHz SPAN	1.552 GHz		1.648 GHz
	4.5 GHz Center Frequency			
	4 GHz SPAN	3.104 GHz		3.296 GHz
	8 GHz SPAN	6.208 GHz		6.592 GHz
	<R3271 ONLY>			
	10 GHz Center Frequency			
	10 MHz SPAN	7.76 MHz		8.24 MHz
	100 MHz SPAN	77.6 MHz		82.4 MHz
	1 GHz SPAN	776 MHz		824 MHz
	2 GHz SPAN	1.552 GHz		1.6484 GHz
	17 GHz Center Frequency			
	10 MHz SPAN	7.76 MHz		8.24 MHz
	100 MHz SPAN	77.6 MHz		82.4 MHz
	1 GHz SPAN	776 MHz		824 MHz
	2 GHz SPAN	1.552 GHz		1.648 GHz
	10 GHz Center Frequency			
	5 GHz SPAN	3.88 GHz		4.12 GHz
	10 GHz SPAN	7.76 GHz		8.24 GHz
	19 GHz SPAN	15.52 GHz		16.48 GHz

Table 4-32 Performance Test Record (4 of 12)

Para. No.	Test Description	Results		
		Min.	Actual	Max.
6	Frequency Span Accuracy (cont'd)			
	LOG Span Accuracy			
	100 MHz Start Frequency			
	200 MHz TR4515 FREQ	179 MHz		221 MHz
	500 MHz TR4515 FREQ	449 MHz		551 MHz
	800 MHz TR4515 FREQ	719 MHz		881 MHz
	10 MHz Start Frequency			
	20 MHz TR4515 FREQ	17 MHz		23 MHz
	50 MHz TR4515 FREQ	44 MHz		56 MHz
	80 MHz TR4515 FREQ	71 MHz		89 MHz
	100 MHz TR4515 FREQ	89 MHz		111 MHz
	200 MHz TR4515 FREQ	179 MHz		221 MHz
	500 MHz TR4515 FREQ	449 MHz		551 MHz
	800 MHz TR4515 FREQ	719 MHz		881 MHz
	1 MHz Start Frequency			
	10 MHz TR4515 FREQ	8 MHz		12 MHz
	20 MHz TR4515 FREQ	17 MHz		23 MHz
	50 MHz TR4515 FREQ	44 MHz		56 MHz
	80 MHz TR4515 FREQ	71 MHz		89 MHz
	100 MHz TR4515 FREQ	89 MHz		111 MHz
	200 MHz TR4515 FREQ	179 MHz		221 MHz
	500 MHz TR4515 FREQ	449 MHz		551 MHz
	800 MHz TR4515 FREQ	719 MHz		881 MHz
7	Resolution Bandwidth Accuracy and Selectivity			
	Resolution Bandwidth Accuracy			
	3 MHz	2.25 MHz		3.75 MHz
	1 MHz	850 kHz		1.15 MHz
	300 kHz	255 kHz		345 kHz
	100 kHz	85 kHz		115 kHz
	30 kHz	25.5 kHz		34.5 kHz
	10 kHz	8.5 kHz		11.5 kHz
	3 kHz	2.55 kHz		3.45 kHz
	1 kHz	850 Hz		1150 Hz
	300 Hz	255 Hz		345 Hz
	100 Hz	85 Hz		115 Hz
	30 Hz	22.5 Hz		37.5 Hz
	100 Hz Digital IF	50 Hz		150 Hz
	30 Hz Digital IF	15 Hz		45 Hz
	10 Hz Digital IF	5 Hz		15 Hz

Table 4-32 Performance Test Record (5 of 12)

Para. No.	Test Description	Results		
		Min.	Actual	Max.
7	Resolution Bandwidth Accuracy and Selectivity (cont'd)			
	Resolution Bandwidth Selectivity			
	3 MHz			15
	1 MHz			15
	300 kHz			15
	100 kHz			15
	30 kHz			15
	10 kHz			15
	3 kHz			15
	1 kHz			15
	300 Hz			15
	100 Hz			15
	30 Hz			20
	100 Hz Digital IF			5 (nominal)
	30 Hz Digital IF			5 (nominal)
	10 Hz Digital IF			5 (nominal)
8	Resolution Bandwidth Switching Uncertainty			
	3 MHz	−0.3 dB		+0.3 dB
	1 MHz	−0.3 dB		+0.3 dB
	300 kHz	−0.3 dB		+0.3 dB
	100 kHz	−0.3 dB		+0.3 dB
	30 kHz	−0.3 dB		+0.3 dB
	10 kHz	−0.3 dB		+0.3 dB
	3 kHz	−0.3 dB		+0.3 dB
	1 kHz	−0.3 dB		+0.3 dB
	300 Hz	−0.3 dB		+0.3 dB
	100 Hz	−0.3 dB		+0.3 dB
	30 Hz	−1.0 dB		+1.0 dB
	100 Hz Digital IF	−1.5 dB		+1.5 dB
	30 Hz Digital IF	−1.5 dB		+1.5 dB
	10 Hz Digital IF	−1.5 dB		+1.5 dB

Table 4-32 Performance Test Record (6 of 12)

Para. No.	Test Description	Results		
		Min.	Actual	Max.
9	Displayed Average Noise Level			
	<R3265 ONLY>			
	1 kHz			−95.23 dBm
	10 kHz			−95.23 dBm
	100 kHz			−96.23 dBm
	1.1 MHz			−120.23 dBm
	10.1 MHz			−125.21 dBm
	101 MHz			−125.07 dBm
	501 MHz			−124.45 dBm
	1001 MHz			−123.68 dBm
	1.5 GHz			−122.90 dBm
	2.0 GHz			−122.13 dBm
	2.5 GHz			−121.35 dBm
	3.0 GHz			−120.58 dBm
	3.5 GHz			−119.80 dBm
	3.5 GHz to 8 GHz			−120.23 dBm
	24 MHz (Low Noise)			−145.00 dBm
	<R3271 ONLY>			
	1 kHz			−95.23 dBm
	10 kHz			−95.23 dBm
	100 kHz			−96.23 dBm
	1.1 MHz			−120.23 dBm
	10.1 MHz			−120.21 dBm
	101 MHz			−120.07 dBm
	501 MHz			−119.45 dBm
	1001 MHz			−118.68 dBm
	1.5 GHz			−117.90 dBm
	2.0 GHz			−117.13 dBm
	2.5 GHz			−116.35 dBm
	3.0 GHz			−115.58 dBm
	3.5 GHz			−114.80 dBm
	3.5 GHz to 7.5 GHz			−115.23 dBm
	7.5 GHz to 15.4 GHz			−108.23 dBm
	15.2 GHz to 23.3 GHz			−101.23 dBm
	23 GHz to 26.5 GHz			−95.23 dBm

Table 4-32 Performance Test Record (7 of 12)

Para. No.	Test Description	Results		
		Min.	Actual	Max.
10	Gain Compression			
	<R3265 ONLY>			
	10.5 MHz	−10 dBm		
	200.5 MHz	−5 dBm		
	3600.5 MHz	−5 dBm		
	<R3271 ONLY>			
	10.5 MHz	−5 dBm		
	200.5 MHz	−5 dBm		
	3600.5 MHz	−5 dBm		
11	Residual Response			
	1 MHz to 3.6 GHz			−100 dBm
	3.5 GHz to 7.5 GHz			−90 dBm
12	Second Harmonic Distortion			
	INPUT FREQ: 1.5 GHz			−70 dBc
	INPUT FREQ: 1.9 GHz			−100 dBc
13	Third Order Intermodulation Distortion			
				(Mixer Input Level : -20dBm)
	<R3265 ONLY>			
	10.5 MHz			−40 dBc
	205 MHz			−50 dBc
	3600 MHz			−55 dBc
	<R3271 ONLY>			
	10.5 MHz			−50 dBc
	3600 MHz			−55 dBc
14	Image, Multiple, and Out-of-Band Response			
	Maximum Response Amplitude			
	<R3265 ONLY>			
	10 MHz to 8 GHz			−70 dBc
	<R3271 ONLY>			
	10 MHz to 18 GHz			−70 dBc
	10 MHz to 23 GHz			−60 dBc
	10 MHz to 26.5 GHz			−50 dBc

Table 4-32 Performance Test Record (8 of 12)

Para. No.	Test Description	Results		
		Min.	Actual	Max.
15	Frequency Response			
	<R3265 ONLY>			
	100 MHz to 3.6 GHz	−1.5 dB		+1.5 dB
	50 MHz to 2.6 GHz	−1.0 dB		+1.0 dB
	3.5 GHz to 7.5 GHz	−1.5 dB		+1.5 dB
	7.4 GHz to 8 GHz	−1.5 dB		+1.5 dB
	<R3271 ONLY>			
	100 MHz to 3.6 GHz	−1.5 dB		+1.5 dB
	50 MHz to 2.6 GHz	−1.0 dB		+1.0 dB
	3.5 GHz to 7.5 GHz	−1.5 dB		+1.5 dB
	7.4 GHz to 15.4 GHz	−3.5 dB		+3.5 dB
	15.4 GHz to 23.3 GHz	−4.0 dB		+4.0 dB
	23.0 GHz to 26.5 GHz	−4.0 dB		+4.0 dB
16	IF Gain Uncertainty			
	RBW 1 MHz Attenuation			
	1 dB	−0.5 dB		+0.5 dB
	2 dB	−0.5 dB		+0.5 dB
	3 dB	−0.5 dB		+0.5 dB
	4 dB	−0.5 dB		+0.5 dB
	5 dB	−0.5 dB		+0.5 dB
	6 dB	−0.5 dB		+0.5 dB
	7 dB	−0.5 dB		+0.5 dB
	8 dB	−0.5 dB		+0.5 dB
	9 dB	−0.5 dB		+0.5 dB
	10 dB	−0.5 dB		+0.5 dB
	20 dB	−0.5 dB		+0.5 dB
	30 dB	−0.5 dB		+0.5 dB
	40 dB	−0.5 dB		+0.5 dB
	50 dB	−0.7 dB		+0.7 dB
	60 dB	−0.7 dB		+0.7 dB

Table 4-32 Performance Test Record (9 of 12)

Para. No.	Test Description	Results		
		Min.	Actual	Max.
16	IF Gain Uncertainty (cont'd)			
	RBW 3 kHz Attenuation			
	1 dB	−0.5 dB		+0.5 dB
	2 dB	−0.5 dB		+0.5 dB
	3 dB	−0.5 dB		+0.5 dB
	4 dB	−0.5 dB		+0.5 dB
	5 dB	−0.5 dB		+0.5 dB
	6 dB	−0.5 dB		+0.5 dB
	7 dB	−0.5 dB		+0.5 dB
	8 dB	−0.5 dB		+0.5 dB
	9 dB	−0.5 dB		+0.5 dB
	10 dB	−0.5 dB		+0.5 dB
	20 dB	−0.5 dB		+0.5 dB
	30 dB	−0.5 dB		+0.5 dB
	40 dB	−0.5 dB		+0.5 dB
	50 dB	−0.7 dB		+0.7 dB
	60 dB	−0.7 dB		+0.7 dB
	70 dB	−0.7 dB		+0.7 dB
	RBW 300 kHz Attenuation			
	1 dB	−0.5 dB		+0.5 dB
	2 dB	−0.5 dB		+0.5 dB
	3 dB	−0.5 dB		+0.5 dB
	4 dB	−0.5 dB		+0.5 dB
	5 dB	−0.5 dB		+0.5 dB
	6 dB	−0.5 dB		+0.5 dB
	7 dB	−0.5 dB		+0.5 dB
	8 dB	−0.5 dB		+0.5 dB
	9 dB	−0.5 dB		+0.5 dB
	10 dB	−0.5 dB		+0.5 dB
	20 dB	−0.5 dB		+0.5 dB
	30 dB	−0.5 dB		+0.5 dB
	40 dB	−0.5 dB		+0.5 dB
	50 dB	−0.7 dB		+0.7 dB
	60 dB	−0.7 dB		+0.7 dB

Table 4-32 Performance Test Record (10 of 12)

Para. No.	Test Description	Results		
		Min.	Actual	Max.
17	Scale Fidelity			
	1 dB/div Log Scale Fidelity			
	−1 dB	−0.2 dB		+0.2 dB
	−2 dB	−0.4 dB		+0.4 dB
	−3 dB	−0.6 dB		+0.6 dB
	−4 dB	−0.8 dB		+0.8 dB
	−5 dB	−1.0 dB		+1.0 dB
	−6 dB	−1.0 dB		+1.0 dB
	−7 dB	−1.0 dB		+1.0 dB
	−8 dB	−1.0 dB		+1.0 dB
	−9 dB	−1.0 dB		+1.0 dB
	−10 dB	−1.0 dB		+1.0 dB
	10 dB/div Log Scale Fidelity			
	−10 dB	−1.0 dB		+1.0 dB
	−20 dB	−1.5 dB		+1.5 dB
	−30 dB	−1.5 dB		+1.5 dB
	−40 dB	−1.5 dB		+1.5 dB
	−50 dB	−1.5 dB		+1.5 dB
	−60 dB	−1.5 dB		+1.5 dB
	−70 dB	−1.5 dB		+1.5 dB
	−80 dB	−1.5 dB		+1.5 dB
	−90 dB	−1.5 dB		+1.5 dB
	Linear Scale Fidelity			
	div from Ref Level			
	1	190.06 mV		212.42 mV
	2	167.7 mV		190.06 mV
	3	145.34 mV		167.7 mV
	4	122.98 mV		145.34 mV
	5	100.62 mV		122.98 mV
	6	78.26 mV		100.62 mV
	7	55.9 mV		78.26 mV
	8	33.54 mV		55.9 mV
	9	11.18 mV		33.54 mV
	QP-mode Log Scale Fidelity			
	dB from Ref Level			
	−10 dB	−11 dBm		−9 dBm
	−20 dB	−21 dBm		−19 dBm
	−30 dB	−31 dBm		−29 dBm
	−40 dB	−41 dBm		−39 dBm

Table 4-32 Performance Test Record (11 of 12)

Para. No.	Test Description	Results		
		Min.	Actual	Max.
18	Input Attenuator Accuracy (4 GHz Center Freq) Switching Accuracy			
	20 dB	-2 dB		+2 dB
	30 dB	-2 dB		+2 dB
	40 dB	-2 dB		+2 dB
	50 dB	-2 dB		+2 dB
	60 dB	-2 dB		+2 dB
	70 dB	-2 dB		+2 dB
	Step-to-Step Accuracy			
	20 dB	−1.1 dB		+1.1 dB
	30 dB	−1.1 dB		+1.1 dB
	40 dB	−1.1 dB		+1.1 dB
	50 dB	−1.1 dB		+1.1 dB
	60 dB	−1.1 dB		+1.1 dB
	70 dB	−1.1 dB		+1.1 dB
	<R3271 ONLY> (15 GHz Center Freq) Switching Accuracy			
	20 dB	-2.5 dB		+2.5 dB
	30 dB	-2.5 dB		+2.5 dB
	40 dB	-2.5 dB		+2.5 dB
	50 dB	-2.5 dB		+2.5 dB
	60 dB	-2.5 dB		+2.5 dB
	70 dB	-2.5 dB		+2.5 dB
	Step-to-Step Accuracy			
	20 dB	−1.3 dB		+1.3 dB
	30 dB	−1.3 dB		+1.3 dB
	40 dB	−1.3 dB		+1.3 dB
	50 dB	−1.3 dB		+1.3 dB
	60 dB	−1.3 dB		+1.3 dB
	70 dB	−1.3 dB		+1.3 dB
	(18 GHz Center Freq) Switching Accuracy			
	20 dB	-3.5 dB		+3.5 dB
	30 dB	-3.5 dB		+3.5 dB
	40 dB	-3.5 dB		+3.5 dB
	50 dB	-3.5 dB		+3.5 dB
	60 dB	-3.5 dB		+3.5 dB
	70 dB	-3.5 dB		+3.5 dB

Table 4-32 Performance Test Record (12 of 12)

Para. No.	Test Description	Results		
		Min.	Actual	Max.
18	Input Attenuator Accuracy (cont'd)			
	<R3271 ONLY> Step-to-Step Accuracy			
	20 dB	−1.8 dB		+1.8 dB
	30 dB	−1.8 dB		+1.8 dB
	40 dB	−1.8 dB		+1.8 dB
	50 dB	−1.8 dB		+1.8 dB
	60 dB	−1.8 dB		+1.8 dB
	70 dB	−1.8 dB		+1.8 dB
19	Sweep Time Accuracy			
	50 μs	44.1 μs		46.8 μs
	100 μs	88.2 μs		93.6 μs
	200 μs	177 μs		187 μs
	500 μs	441 μs		468 μs
	1 ms	882 μs		936 μs
	2 ms	1.77 ms		1.87 ms
	5 ms	4.41 ms		4.68 ms
	10 ms	8.82 ms		9.36 ms
	20 ms	17.7 ms		18.7 ms
	50 ms	44.1 ms		46.8 ms
	100 ms	88.2 ms		93.6 ms
	200 ms	177 ms		187 ms
	500 ms	441 ms		468 ms
	1 s	882 ms		936 ms
	2 s	1.77 s		1.87 s
	5 s	4.41 s		4.68 s
	10 s	8.82 s		9.36 s
	20 s	17.7 s		18.7 s
	50 s	44.1 s		46.3 s
	100 s	88.2 s		93.6 s
20	Calibration Amplitude Accuracy	−10.3 dBm		−9.7 dBm

MEMO

5. ADJUSTMENT

5.1 Measurement Standards and Support Test Equipment Performance Requirements

The Minimum Use Specifications (MUS) are the calculated minimum performance specifications criteria needed for the Measurement Standards (MS) and support M&TE to be used for comparison measurement required in the Adjustment Procedure (AP) process.

The MUS is developed through uncertainty analysis and is calculated through assignment of a defined and documented uncertainty/accuracy ratio or margin between the specified tolerances of the UUT and the capability (uncertainty specifications) required of the measurement standards system. The MUS is required to assist a measurement specialist in the evaluation of existing or selected alternate measurement standards equipment.

MS and SM&TE environmental range: Temperature: 18 to 28°C
Relative humidity: 30 to 70%

MS and SM&TE warmup/stabilization period requirements: 60 minutes

Table 5-1 Measurement Standards (MS) Performance Requirements (1 of 2)

Equipment Generic Name (Quantity)	Minimum Use Specifications (MUS)	Manufacturer/Model /Option Applicable
Frequency standard	Output frequency: 10 MHz Stability: 5×10^{-10}/day Output impedance: Approx. 50 Ω Output voltage: 1 Vp-p or more	TR3110
Synthesized sweeper	Frequency range: 10 to 18 MHz Frequency accuracy (CW): 3×10^{-8}/day Power level range: −15 to +15 dBm	TR4515
Frequency synthesizer	Frequency range: 1 to 20 MHz Stability: 5×10^{-6}/year Power level range: −10 to +13 dBm	HP 3325

Table 5-1 Measurement Standards (MS) Performance Requirements (2 of 2)

Equipment Generic Name (Quantity)	Minimum Use Specifications (MUS)	Manufacturer /Model/Option Applicable
Digital multimeter	DC voltage resolution: 5 digits or more	TR6851
Spectrum analyzer	Frequency range: Up to 4.5 GHz	TR4173
Synthesized signal generator	Frequency range: 10 MHz to 4 GHz Residual SSB phase noise: 1 kHz offset < −115 dBc/Hz 10 kHz offset < −125 dBc/Hz 100 kHz offset < −130 dBc/Hz Power level range: −100 to +10 dBm	R4262
Power meter	Accuracy : ±0.02 dB Decibel relative mode	HP436A
Power sensor	Frequency range: 50 MHz to 26.5 GHz Power range: 1 μW to 100 mW Maximum SWR: 1.25 (26.5 GHz)	HP8485A
Power sensor	Frequency range: 10 MHz to 18 GHz Power range: 1 μW to 100 mW	HP8481A
Spectrum analyzer	Frequency range: Up to 100 MHz With built-in TG	R3361B
Sweeper	Frequency range: 10 MHz to 26.5 GHz Power range: −5 to +10 dBm (at 3.0 GHz)	HP8350 and HP83595A
Sweep adapter		TR13211
Frequency comparator	Frequency: 10 MHz 1×10^{-9} frequency detectable	
Impedance generator		R14602

Table 5-2 Support Measuring & Test Equipment (M&TE) Performance Requirements

Equipment Generic Name (Quantity)	Minimum Use Specifications (MUS)	Manufacturer /Model/Option Applicable
Adapter	Type N (male) to BNC (female)	JUG -201A/U (Hirose)
Adapter	Type N (male) to SMA (female)	HRM-554S
Adapter	SMA (male) to SMA (male)	50-673-0000-31 (Selectro)
Adapter	Type N (female) to BNC (male)	NJ-BNCP (DDK)
Adapter	SMA (female) to SMA (female)	HRM-501 (Hirose)
20 dB fixed attenuator	Connector: SMA (male), SMA (female)	AT-120 (Hirose)
Low-pass filter	Cutoff frequency: 2.2 GHz Rejection at 3 GHz: >40 dB Rejection at 3.8 GHz: >80 dB	DEE-001172-1 (Advantest)
Double balanced mixer	Frequency range: 10 to 100 MHz	
Cable	Frequency range: DC to 26.5 GHz Maximum SWR: <1.45 at 26.5 GHz Length: Approx. 70 cm Connector: SMA (male) at both ends	A01002
Cable	Length: 150 cm Connection: BNC (male) at both ends	MI-09
Cable	Length: 10 cm Connection: BNC (male) at both ends	MC-61
Cable	Frequency: 21.4 MHz Length: 100 cm Connector: UM (male), BNC (male)	MC-36A
Probe	Frequency: 21.4 MHz 10:1 Impedance: 10 MHz	P6133 (Tektronix)

5.2 Preliminary Operations

WARNING

Always make sure that the power cord of the spectrum analyzer is plugged into a three-hole grounded outlet or two-hole outlet with the grounded adapter. You can be fatally shocked if you fail to follow this rule.

Do not touch live circuits when adjusting an instrument.

(1) Always confirm that the POWER switch is OFF before connecting the power cord to the AC line.

(2) Before performing any adjustment, allow the instrument to warm up for five minutes.

5.3 Adjustment

5.3.1 A/D Adjustment

- ASSEMBLY ADJUSTMENT
  Log block (WBL-32xxLOG)

- RELATED PORFORMANCE TEST
  There is no related porformance test.

- DESCRIPTION
  The A/D adjustment including offset and gain adjustment of the positive peak detector, negative peak detector, sample mode, FFT mode, and high-speed mode can be made by changing the DAC data and variable resistance. Also, the reference voltage and slope detector can be adjusted by changing the variable resistance.

  [Reference Voltage Adjustment]

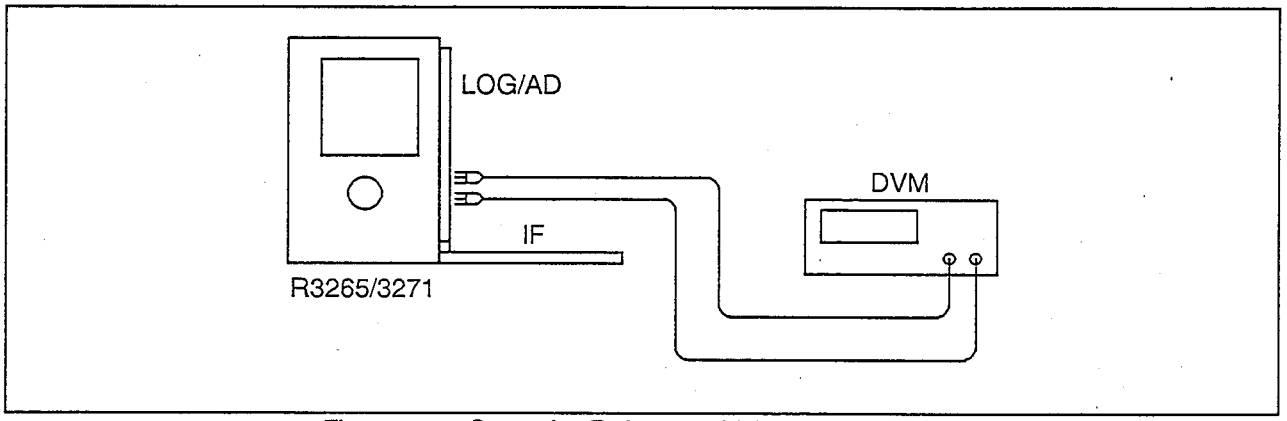


Figure 5-1 Setup for Reference Voltage Adjustment

- EQUIPMENT

DVM	TR6851
Probe	P6133

- PROCEDURE

(1) Turn off the POWER switch of the R3265/3271, unplug the power cord, and remove the system cover. Place the system in the side angle, remove the interface block screws, and open the interface block. Also, remove the top cover (MBS-72887) from the A/D section.
Plug the power cord, and turn the POWER switch on.

(2) Connect the DVM probe between TP1 (GND) and TP3 (REF), and adjust R157 to have +2.000 ±1 mV.

[Adjusting the positive peak detector, negative peak detector, sample mode, FFT mode, and high-speed mode]

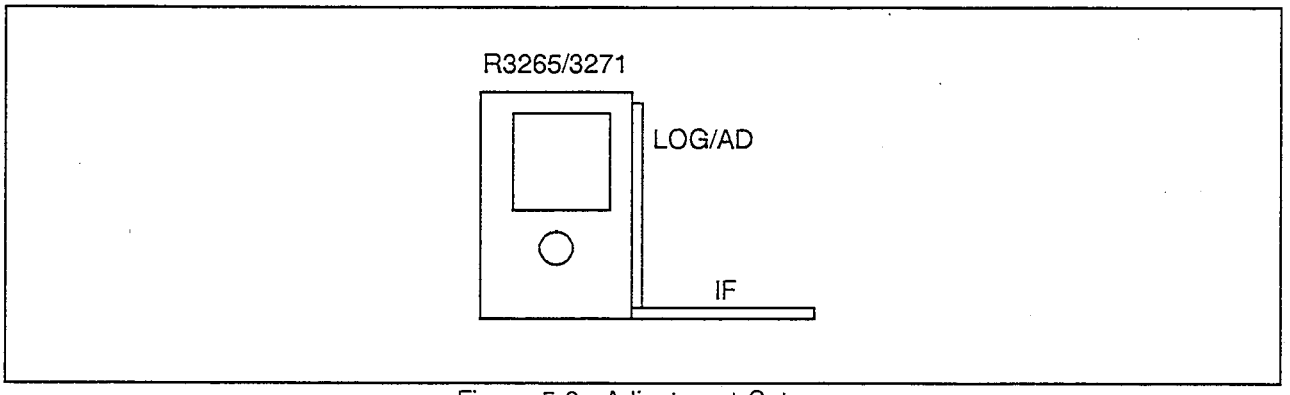


Figure 5-2 Adjustment Setup

- PROCEDURE

(1) Turn off the POWER switch of the R3265/3271, unplug the power cord, and remove the system cover. Place the system in the side angle, remove the interface block screws, and open the interface block. Also, remove the top cover (MBS-72887) from the A/D section.
Plug the power cord, turn the POWER switch on, and warm up the system 30 minutes or more.

(2) Press the [PRESET] key of the R3265/3271, and press the MARKER [ON] key.

(3) Hold down the [SHIFT] key and press the [5] key on the R3265/3271.
When the "Please input password!!" message appears, press [9], [4], [2], [8] and [4] keys in this sequence.

(4) Hold down the [SHIFT] key and press the [REF LEVEL] key.

(5) Press the [A/D] and [X3.52 AMP] keys (to select the Sample mode).

(6) Press the [BOTTOM] key and adjust the data knob to have the marker value of −100.00 ±0.03 dB.

(7) Press the [TOP] key and adjust R84 to have the marker value of 0.00 ±0.03 dB.

(8) Repeat Steps (6) and (7) until the [BOTTOM] and [TOP] values reach −100 ±0.03 dB and 0.00 ±0.03 dB, respectively.

(9) Press the [RETURN] and [POSI-NEGA] keys (to select the Positive-Negative mode).

(10) Press the [P-N1 BOTTOM] key, and adjust the data knob to have the marker value of −100 ±0.03 dB.

(11) Press the [P-N1 TOP] key, and adjust R11 to have the marker value of 0.00 ±0.03 dB.

(12) Repeat Steps (10) and (11) until the [P-N1 BOTTOM] and [P-N1 TOP] values reach −100 ±0.03 dB and 0.00 ±0.03 dB, respectively.

(13) Press the [P-N2 BOTTOM] key, and adjust the data knob to have the marker value of −100 ±0.03 dB.

(14) Press the [RETURN] and [P-P/D] keys. (Positive peak detector)

(15) Press the [P-P/D1 BOTTOM] key, and adjust the data knob to have the marker value of −100 ±0.03 dB.

(16) Press the [P-P/D2 BOTTOM] key, and adjust the data knob to have the marker value of −100 ±0.03 dB.

(17) As the [P-P/D1 BOTTOM] and [P-P/D2 BOTTOM] data are displayed alternately, repeat Steps (15) and (16) until the two lines become a single line.

(18) Press the [P-P/D TOP] key, and adjust R16 so that the marker value variation comes within ±0.03 dB.

(19) Press the [RETURN] and [N-P/D] keys. (Negative peak detector)

(20) Press the [BOTTOM] key, and adjust the data knob to have the marker value of −100 ±0.03 dB.

(21) Press the [TOP] key, and adjust R42 to have the marker value of 0.00 ±0.03 dB.

(22) Repeat Steps (20) and (21) until the [BOTTOM] and [TOP] −100 ±0.03 dB and 0.00 ±0.03 dB, respectively.

(23) Press the [RETURN] and [FFT] keys (to select the FFT mode).

(24) Press the [0 dB BOTTOM] key, and adjust the data knob to have the marker value of −31.25 ±0.03 dB.

(25) Press the [0 dB TOP] key, and adjust R67 to have the marker value of −68.75 ±0.03 dB.

(26) Repeat Steps (24) and (25) until the [0 dB BOTTOM] and [0 dB TOP] values reach −31.25 ±0.03 dB and −68.75 ±0.03 dB, respectively.

(27) Press the [20 dB BOTTOM] key, and adjust the data knob so that the on-screen messages have the highest brightness.

(28) Press the [RETURN] and [HIGH A/D] keys (to select the high-speed mode).

(29) Press the [BOTTOM] key, and adjust the data knob to have the marker value of −100 ±0.00 dB.

(30) Press the [TOP] key, and adjust the data knob to have the marker value of 0.00 ±0.00 dB.

(31) Repeat Steps (29) and (30) until the [BOTTOM] and [TOP] values reach −100 ±0.00 dB and 0.00 ±0.00 dB, respectively.

(32) Press the [RETURN], [SHIFT], MARKER and [ON] keys (to write data in the EEPROM).

[Slope Detector Adjustment]

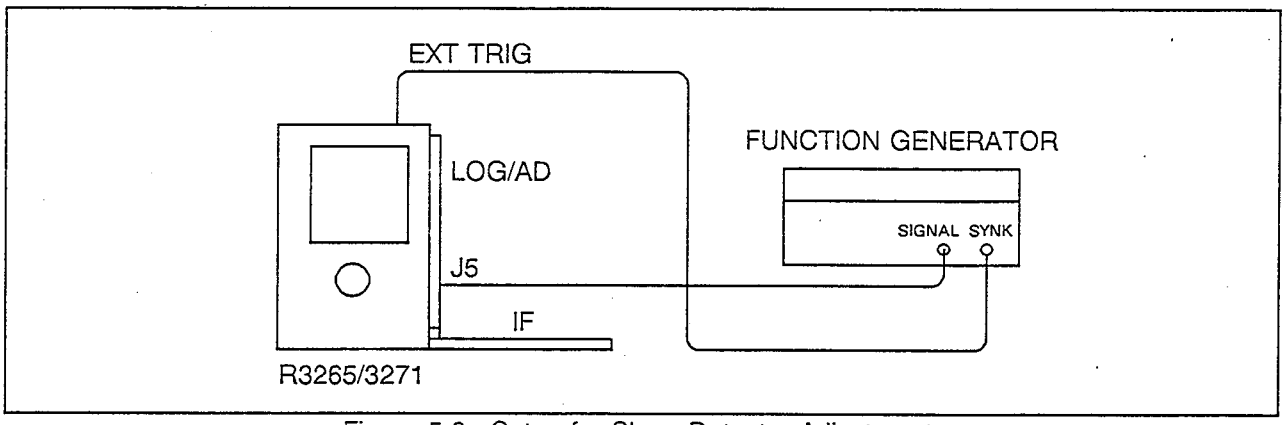


Figure 5-3 Setup for Slope Detector Adjustment

- EQUIPMENT

  Function generator HP3325A
  Cable ..... MI-09; BNC (male), 150 cm long

(1) Turn off the POWER switch of the R3265/3271, unplug the power cord, and remove the system cover. Place the system in the side angle, remove the interface block screws, and open the interface block.
Plug the power cord, turn the POWER switch on, and warm up the system 30 minutes or more.

(2) Connect the BNC cable between the EXT TRIG terminal and SYNC OUT terminal of the HP3325A on the R3265/3271 rear panel.

(3) Connect the signal cable between J5 of the AD block and SIGNAL terminal of HP3325A.

(4) Press the [PRESET] key of the R3265/3271, and set the controls as follows:
FREQ SPAN ..... ZERO SPAN
TRIG ..... EXT

(5) Hold down the [SHIFT] key and press the [BK SP] key of the R3265/3271 to select the Debug mode. Then, press the following keys in this sequence.
[3] [1] [5] [0] [0] [0] [ENTER] [1] [2] [ENTER]
Press the [RETURN] key to exit the Debug mode.

(6) Set the HP3325A as follows:

FREQ	50 Hz (SINE)
AMPTD	900 mV
DC OFFSET	500 mV

(7) Adjust R111 so that the smooth waveforms are displayed on the screen.

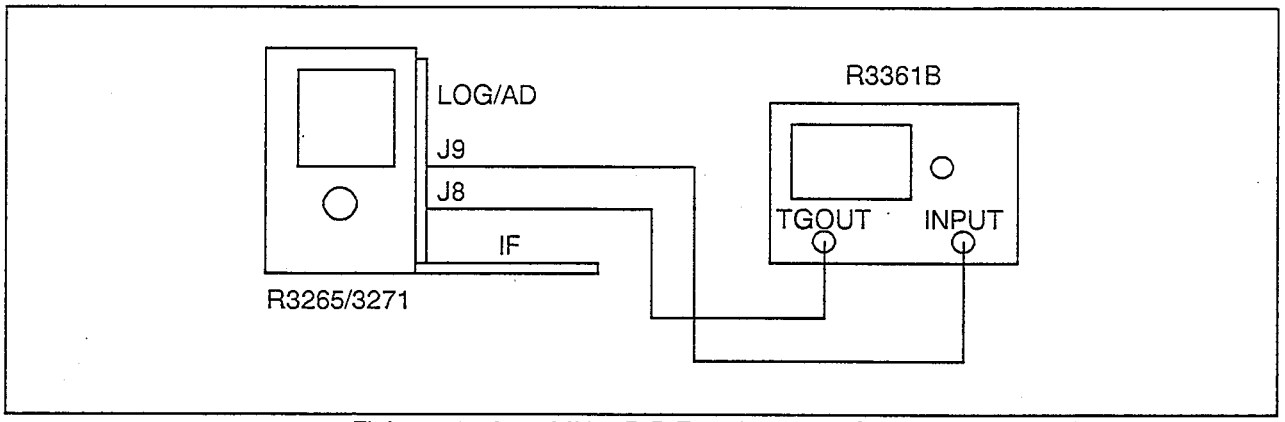
5.3.2 Log Amp Adjustment

- ASSEMBLY ADJUSTMENT
  Log block (WBL-32xxLOG)

- RELATED PERFORMANCE TEST
  Scale fidelity

- DESCRIPTION
  The Log Amp can be adjusted for 21.4 MHz BPF by changing the coil and variable resistor values. The LOG/LIN GAIN, OFFSET, MAG AMP, STEP AMP, and QP DET values can be adjusted by changing the DAC data.

[21.4 MHz BPF Adjustment]



Figire 5-4 21.4 MHz B.P.F. Adjustment Setup

- EQUIPMENT

Spectrum analyzer with TG	R3361B
Cable	MI-09; BNC (male), 150 cm long

- PROCEDURE

(1) Turn off the POWER switch of the R3265/3271, unplug the power cord, and remove the system cover. Place the system in the side angle, remove the interface block screws, and open the interface block.
Plug the power cord, turn the POWER switch on, and warm up the system 30 minutes or more.

(2) Connect the signal cable between J8 of the LOG block and the TG OUT terminal of R3361. Also, connect the cable between J9 of the LOG block and the INPUT terminal of R3361.

(3) Press the [PRESET] key of the R3265/3271, and set the controls as follows:

CENTER FREQ	0 MHz
FREQ SPAN	10 MHz
VBW	1 kHz

(4) Press the [PRESET] and [TG] keys of R3361B, and set the controls as follows:

CENTER FREQ	21.42 MHz
FREQ SPAN	5 MHz
TG LEVEL	−10 dBm
dB/DIV	1 dB/DIV

(5) Hold down the [SHIFT] key and press the [BK SP] key of the R3265/3271 to select the Debug mode. Then, press the following keys in this sequence.

[4] [1] [0] [2] [7] [0] [ENTER] [0] [7] [ENTER]

(6) Adjust L14 so that the peak of waveforms comes at the center of the screen on the R3361B.

(7) Press the following keys in this sequence on the R3265/3271:

[4] [1] [0] [2] [7] [0] [ENTER] [2] [7] [ENTER]

(8) Press the [B] [WRITE B], and [VIEW B] keys on the R3361 to store the waveforms.

(9) Press the following keys in this sequence on the R3265/3271:

[4] [1] [0] [2] [7] [0] [ENTER] [0] [7] [ENTER]

(10) Adjust R239 so that the peak of the waveforms on the R3361B reaches the same level as that stored in [B] .

(11) Repeat Steps (7) to (10) so that they have the same level.

[MAG AMP Adjustment]

- PROCEDURE

(1) Turn on the POWER switch of the R3265/3271 and warm up it 30 minutes or more.

(2) Press the [PRESET] key of the R3265/3271 and set the controls as follows:

CENTER FREQ	0 MHz
FREQ SPAN	10 kHz
VBW	1 kHz
MARKER	ON

(3) Hold down the [SHIFT] key and press the [5] key on the R3265/3271. When the "Please input password!!" message appears, press the [9], [4], [2], [8] and [4] keys in this sequence.

(4) Hold down the [SHIFT] key and press the [PEF LEVEL] key.

(5) Press the [LOG] and [MAG ADJ] keys.

(6) Press the [MAG 10/5 dB.A] key, and adjust the data knob to have the marker value of −100.00 dBm ±0.2 dB.

(7) Press the [MAG 10/5 dB.B] key, and adjust the data knob to have the marker value of 0.00 dBm ±0.2 dB.

(8) Press the [LIN ×1, ×2.A] key and enter the same value as the MAG 5dB.A data.

(9) Press the [LIN ×1, ×2.B] key and enter the same value as the MAG 5dB.A data.

(10) Press the [NEXT MENU] and [MAG 2 db.A] key, and adjust the data knob to have the marker value of −100.00 dBm ±0.2 dB.

(11) Press the [MAG 2 dB.B] key, and adjust the data knob to have the marker value of 0.00 dBm ±0.2 dB.

(12) Press the [MAG 1 dB.A] key, and adjust the data knob to have the marker value of −100.00 dBm ±0.2 dB.

(13) Press the [MAG 1 dB.B] key, and adjust the data knob to have the marker value of 0.00 dBm ±0.2 dB.

(14) Press the RETURN, SHIFT, MARKER and ON keys (to write data in the EEPROM).

[LOG/LIN GAIN, OFFSET, STEP AMP, and QP Adjustment]

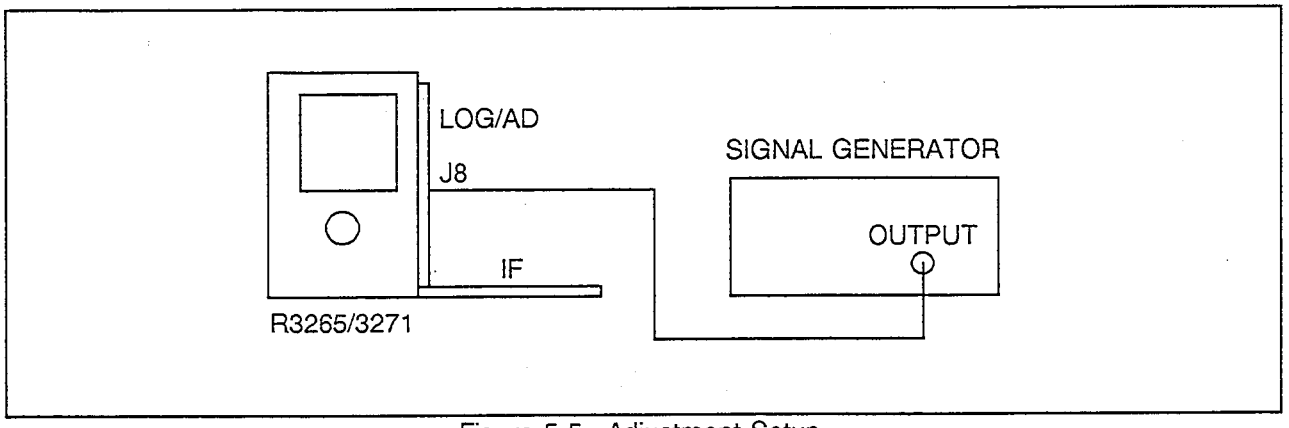


Figure 5-5 Adjustment Setup

- EQUIPMENT

  Signal generator R4262
  Cable ..... MI-09; BCN (male), 150 cm long

- PROCEDURE

(1) Turn off the POWER switch of the R3265/3271, unplug the power cord, and remove the system cover. Place the system in the side angle, remove the interface block screws, and open the interface block.
Plug the power cord, turn the POWER switch on, and warm up the system 30 minutes or more.

(2) Connect the signal cable between J8 of the LOG block and the OUTPUT terminal of R4262.

(3) Set the R4262 as follows:

FREQ ..... 21.42 MHz

(4) Press the [PRESET] key of the R3265/3271, and set the controls as follows:

CENTER FREQ	0 MHz
FREQ SPAN	10 MHz
VBW	1 kHz
MARKER	ON

(5) Hold down the [SHIFT] key and press the [5] key on the R3265/3271. When the "Please input password!!" message appears, press the [9], [4], [2], [8] and [4] keys in this sequence.

(6) Hold down the [SHIFT] key and press the [REF LEVEL] key.

(7) Press the [LOG] key.

(8) Set the AMPLITUDE of R4262 to 0 dBm.

(9) Press the [GAIN ADJ] and [LOG] keys, and adjust the data knob to have the marker value of 0.00 dBm ±0.2 dB.

(10) Set the AMPLITUDE of R4262 to −90 dBm.

(11) Press the [RETURN] and [LOG OFFSET] keys, and adjust the data knob to have the marker value of −90.00 dBm ±0.2 dB.

(12) Repeat Steps (12) to (15) so that the [LOG] and [LOG OFFSET] values become 0.00 dBm ±0.2 dB and −90.00 dBm ±0.2 dB, respectively.

(13) Press the [RETURN], [GAIN ADJ], [LIN] keys in this sequence.

(14) Set the AMPLITUDE of R4262 to 0 dBm.

(15) Adjust the data knob to have the marker value of 0.00 dBm ±0.2 dB.

(16) Set the AMPLITUDE of R4262 to −10 dBm.

(17) Press the [LIN 10 dB] key, and adjust the data knob to have the marker value of 0.00 dBm ±0.2 dB.

(18) Set the AMPLITUDE of R4262 to −20 dBm.

(19) Press the [LIN 20 dB] key, and adjust the data knob to have the marker value of 0.00 dBm ±0.2 dB.

(20) Set the AMPLITUDE of R4262 to −30 dBm.

(21) Press the [LIN 30 dB] key, and adjust the data knob to have the marker value of 0.00 dBm ±0.2 dB.

(22) Set the AMPLITUDE of R4262 to −40 dBm.

(23) Press the [NEXT MENU] and [LIN 40 dB] keys, and adjust the data knob to have the marker value of 0.00 dBm ±0.2 dB.

(24) Set the AMPLITUDE of R4262 to −50 dBm.

(25) Press the [LIN 50 dB] key, and adjust the data knob to have the marker value of 0.00 dBm ±0.2 dB.

(26) Set the AMPLITUDE of R4262 to −60 dBm.

(27) Press the [LIN 60 dB] key, and adjust the data knob to have the marker value of 0.00 dBm ±0.2 dB.

(28) Set the AMPLITUDE of R4262 to −70 dBm.

(29) Press the [LIN 70 dB] key, and adjust the data knob to have the marker value of 0.00 dBm ±0.2 dB.

(30) Set the AMPLITUDE of R4262 to −80 dBm.

(31) Press the [LIN 80 dB] key, and adjust the data knob to have the marker value of 0.00 dBm ±1 dB.

(32) Press the [RETURN], [SHIFT], MARKER and [ON] keys (to write data in the EEPROM).

(33) Press the [QP], [QP ZERO ADJ], [QP GAIN ADJ] and [QP OFFSET] keys in this sequence.

(34) Set the AMPLITUDE of R4262 to 0 dBm.

(35) Adjust the data knob to have the marker value of 0.00 dBm ±0.2 dB.

(36) Set the AMPLITUDE of R4262 to −20 dBm.

(37) Press the [QP GAIN ADJ] key, and adjust the data knob to have the marker value of −40.00 dBm ±0.5 dB.

(38) Set the AMPLITUDE of R4262 to −40 dBm.

(39) Press the [QP ZERO ADJ] key, and adjust the data knob to have the marker value of −80.00 dBm ±0.5 dB.

(40) Repeat Steps (36) to (41) so that the [QP OFFSET], [QP GAIN ADJ] and [QP ZERO ADJ] values. become 0.00dBm ±0.2dB, −40.00dBm ±0.5dB, and −80.00dBm ±0.5dB, respectively.

(41) Press the [RETURN], [SHIFT], MARKER and [ON] keys (to write data in the EEPROM)

(42) Set the AMPLITUDE of R4262 to 0 dBm.

(43) Press the [STEP AMP ADJ] and [OFF] keys, and record the marker value.

(44) Set the AMPLITUDE of R4262 to −10 dBm.

(45) Press the [STEP 10 dB] key, and adjust the data knob so that the marker value reaches the value recorded in Step (47) subtracted by −10 dBm ±0.2 dB.

(46) Set the AMPLITUDE of R4262 to −20 dBm.

(47) Press the [STEP 20 dB] key, and adjust the data knob so that the marker value reaches the value recorded in Step (47) subtracted by −20 dBm ±0.2 dB.

(48) Set the AMPLITUDE of R4262 to −30 dBm.

(49) Press the [STEP 30 dB] key, and adjust the data knob so that the marker value reaches the value recorded in Step (47) subtracted by −30 dBm ±0.2 dB.

(50) Set the AMPLITUDE of R4262 to −40 dBm.

(51) Press the [STEP 40 dB] key, and adjust the data knob so that the marker value reaches the value recorded in Step (47) subtracted by −40 dBm ±0.2 dB.

(52) Set the AMPLITUDE of R4262 to −50 dBm.

(53) Press the [NEXT MENU], [STEP 50 dB] keys, and adjust the data knob so that the marker value reaches the value recorded in Step (47) subtracted by −50 dBm ±0.2 dB.

(54) Set the AMPLITUDE of R4262 to −60 dBm.

(55) Press the [STEP 60 dB] key, and adjust the data knob so that the marker value reaches the value recorded in Step (47) subtracted by −60 dBm ±0.2 dB.

(56) Set the AMPLITUDE of R4262 to −70 dBm.

(57) Press the [STEP 70 dB] key, and adjust the data knob so that the marker value reaches the value recorded in Step (47) subtracted by −70 dBm ±0.2 dB.

(58) Set the AMPLITUDE of R4262 to −80 dBm.

(59) Press the [STEP 80 dB] key, and adjust the data knob so that the marker value reaches the value recorded in Step (47) subtracted by −80 dBm ±0.2 dB.

(60) Press the [RETURN], [SHIFT], MARKER and [ON] keys (to write data in the EEPROM).

5.3.3 IF Filter Adjustment

- ASSEMBLY ADJUSTED
  IF block (WBL-32xxIF)

- RELATED PERFORMANCE TEST
  Resolution bandwidth accuracy and selectivity

- DESCRIPTION
  The IF filter consists of the 4-stage band-pass filter of the LC and the 8-stage band-pass filter of the resonator (4-stage lithium tantalum and 4-stage crystal filters). The IF filter can easily be adjusted by observing the filter waveforms on the spectrum analyzer having the TG.

[LC Filter Adjustment]

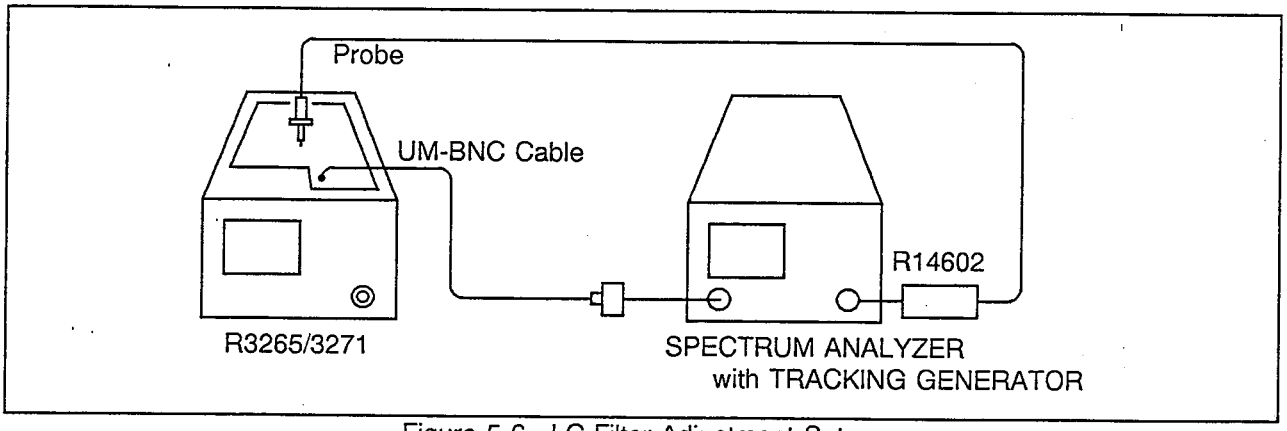


Figure 5-6 LC Filter Adjustment Setup

- EQUIPMENT

Spectrum analyzer with TG	R3361A/B
Impedance converter	R14602
Probe	P6133
Adapter:	
Type N (male) to BNC (female)	JUG-201A/U
Cable:	
UM-BNC, 100 cm long	MC-36A

- PROCEDURE

(1) Turn off the POWER switch of the R3265/3271, unplug the power cord, and remove the system cover. Then, remove the top cover from the interface block (WBL-32xxIF). Plug the power cord, turn the POWER switch on, and warm up the system 30 minutes or more.

(2) Connect the UM-BNC cable (and N-BNC conversion adapter) between J1 of the IF block and TG OUTPUT of the R3361. Connect the probe to the INPUT terminal of R3361 using the R14602 impedance converter.

(3) Press the [RESET] key of the R3361 and set the controls as follows:

CENTER FREQ	21.4205 MHz
SPAN	1 MHz
REF. LEVEL	−15 dBm
SCALE	1 dB/div
TG LEVEL	10 dBm

(4) Press the [RESET] key of the R3265/3271, hold down the [SHIFT] key and press [CAL 7] key to set the [CAL CORR ON/OFF] switch to OFF.
Then, press the [CPL] and [RBW] keys to set the RBW to 300 kHz.

(5) Connect the probe connected to the R3361 to TP16 of the IF block.

(6) Adjust L62 so that the peak of waveforms reaches the center of the screen on the R3361.

(7) Connect the probe to TP17, and adjust L64 in the same way as for Step (6).

(8) Connect the probe to TP18, and adjust L68 in the same way as for Step (6).

(9) Connect the UM-BNC cable (and N-BNC conversion adapter) between J5 of the IF block and the INPUT terminal of the R3361.

(10) Set the REF LEVEL of the R3361 to 0 dBm.

(11) Adjust L70 in the same way as for Step (6).

[Resonator Filter Adjustment]

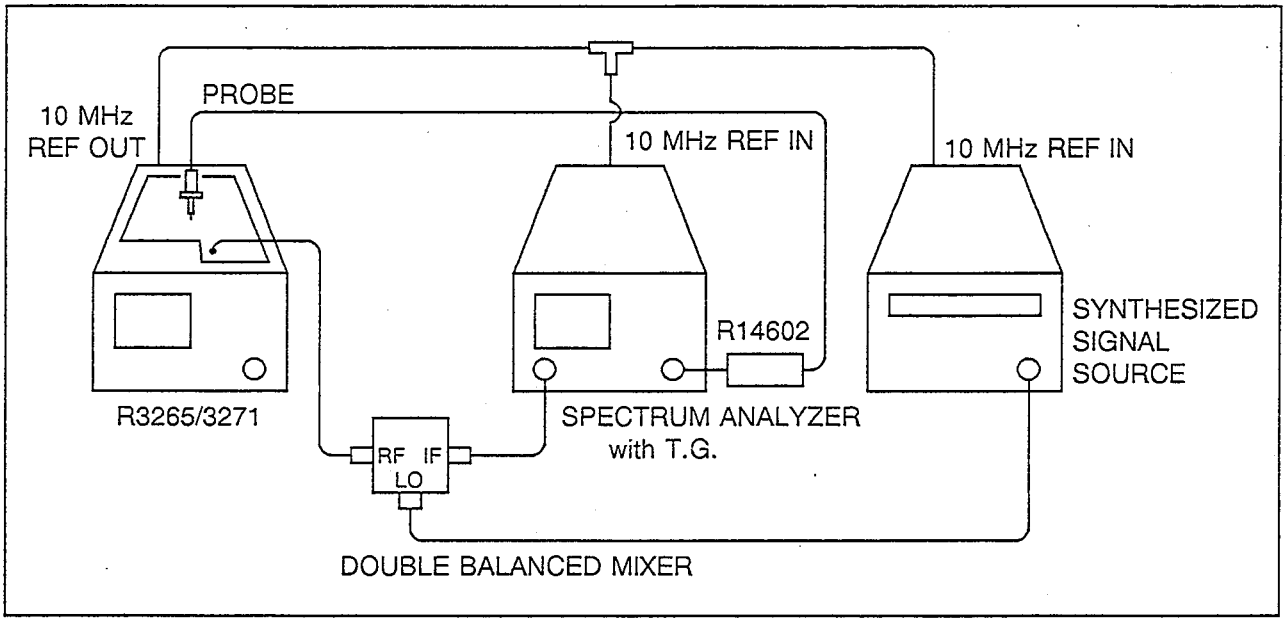


Figure 5-7 Resonator Filter Adjustment Setup

- EQUIPMENT

Spectrum analyzer with TG	R3361A/B
Synthesized signal source	TR4515
Double balanced mixer	Frequency range: 10 to 100 MHz
Probe	P6133
Cable	MI-09; BNC (male), 150 cm long
Impedance converter	R14602
Coaxial cable and others for mixer connection	

- PROCEDURE

Adjustment of lithium tantalum filter:

(1) Turn off the POWER switch of the R3265/3271, unplug the power cord, and remove the system cover. Then, remove the top cover from the interface (IF) block.
Plug the power cord, turn the POWER switch on, and warm up the system 30 minutes or more.

(2) Connect the BNC cables between the 10 MHz REF IN/OUT terminal of R3265/3271, 10 MHz REF terminal of R3361, and the EXT 10 MHz terminal of TR4515. Also, connect the TG of R3361 to the IF port of the double balanced mixer. Connect the OUTPUT terminal of TR4515 to the LO port of the double balanced mixer. Connect the J1 terminal of IF block of the R3265/3271 to the RF port of the double balanced mixer. Connect the probe to the INPUT terminal of R3361 using the R14602 impedance converter.

(3) Press the [PRESET] key of the R3265/3271, hold down the [SHIFT] key and press [CAL 7] key to set the [CAL CORR ON/OFF] to OFF.
Also, press the [PRESET] key of the R3361, and set the controls as follows:

CENTER FREQ	3.5795 MHz
SPAN	0 Hz
REF. LEVEL	−25 dBm
SCALE	1 dB/div
TG LEVEL	−10 dBm
RBW	100 Hz
10 MHz REF	EXT IN

Press the [PRESET] key of the TR4515, and set the controls as follows:

CW FREQ	25 MHz
LEVEL	+10 dBm
10 MHz REF	EXT IN

(4) Press the [CPL] and [RBW] keys of the R3265/3271 to set the RBW to 3 kHz.

(5) Connect the prove from R3361 to TP6.

(6) Adjust C43 of the IF block to have the highest display level of R3361.

(7) Adjust C57 in the same way as for Step (6).

(8) Repeat Steps (6) and (7) to have the highest display level of R3361.

(9) Connect the probe to TP11.

(10) Adjust C110 of the IF block to have the highest display level of R3361.

(11) Adjust C123 in the same way as for Step (10).

(12) Repeat Steps (10) and (11) to have the highest display level of R3361.

(13) Set the SPAN of R3361 to 500 kHz, and set RBW to AUTO.

(14) Set the RBW of R3265/3271 to 100 kHz.

(15) Connect the probe to TP5.

(16) Set the R3361 to 10 dB/div, and adjust C41 so that the right and left sides of waveforms have the same signal level on the screen.

(17) Set the R3361 to 1 dB/div, and adjust L18 so that the peak of the waveforms comes to the center of the screen.

(18) Connect the probe to TP6, and adjust C55 in the same way as for Step (16). Also, adjust L22 in the same way as for Step (17).

(19) Connect the probe to TP10, and adjust C108 in the same way as for Step (16). Also, adjust L36 in the same way as for Step (17).

(20) Connect the probe to TP11, and adjust C121 in the same way as for Step (16). Also, adjust L40 in the same way as for Step (17).

[Crystal Filter Adjustment]

(1) Perform Steps (1) to (3) of the lithium tantalum filter adjustment.

(2) Set the RBW of R3265/3271 to 10 Hz.

(3) Connect the probe to TP8.

(4) Adjust C75 to have the highest display level of R3361.

(5) Adjust C85 in the same way as for Step (4).

(6) Repeat Steps (4) and (5) to have the highest display level of R3361.

(7) Connect the probe to TP13.

(8) Adjust C137 and C149 in the same way as for Steps (4) to (6).

(9) Set the RBW of R3265/3271 to 1 kHz.

(10) Connect the probe to TP7.

(11) Set the SPAN of R3361 to 2 kHz, and set its SCALE to 10 dB/div. Also, adjust C71 so that the right and left sides of waveforms have the same signal level on the screen.

(12) Set the SPAN of R3361 to 2 kHz, and set its SCALE to 1 dB/div. Also, adjust L26 so that the peak of waveforms comes to the center of the screen.

(13) Connect the prove to TP8, and adjust C83 in the same way as for Step (11). Also, adjust L30 in the same way as for Step (12).

(14) Connect the probe to TP12, and adjust C135 in the same way as for Step (11). Also, adjust L44 in the same way as for Step (12).

(15) Connect the probe to TP13, and adjust C147 in the same way as for Step (11). Also, adjust L48 in the same way as for Step (12).

5.3.4 IF Step Amp Adjustment

- ASSEMBLY ADJUSTED
  IF block (WBL-32xxIF)

- RELATED PERFORMANCE TEST
  IF gain uncertainty test

- DESCRIPTION
  The IF step amp consists of two 10dB amps and four 20dB amps. In addition, it contains the 10dB amp that is used for the R3265 in the Low Noise mode. These amplifier gains can be adjusted using the variable resistors. If the amp has the 10dB gain, it must be adjusted so that its output level matches the original one when the CAL Signal Level is reduced for 10 dB. Also, if the amp has the 20dB gain, it must be adjusted so that the output level matches the original one when the CAL Signal Level is reduced for 20 dB.

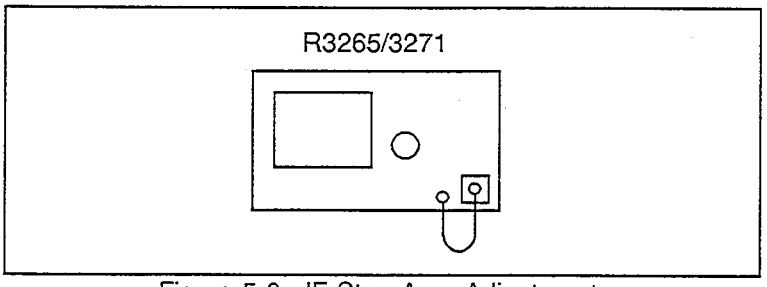


Figure 5-8 IF Step Amp Adjustment

- EQUIPMENT

Cable	MC-61; BNC (male), 10 cm long
Adapter	JUG-201A/U; type N (male) to BNC (female)

- PROCEDURE

(1) Turn off the POWER switch of the R3265/3271, unplug the power cord, and remove the system cover. Plug the power cord, turn the POWER switch on, and warm up the system 30 minutes or more.

(2) Connect the BNC cable (using the N-BNC conversion adapter) between the CAL OUT and INPUT terminals of the R3265/3271.

(3) Press the [PRESET] key of the R3265/3271, and set the controls as follows:

CENTER FREQ	25 MHz
SPAN	0 Hz
REF. LEVEL	−5 dBm
SCALE	1 dB/div
RBW	100 kHz

(4) Make sure that approximately −10 dBm of signals are displayed on the screen.
Then, press the following keys in this sequence.
[B], [WRITE B] [VIEW B] MARKER [ON], [NEXT MENU], [DSP POSI UP/LOW], [PREV MENU], [⊿ MKR], [A].

(5) Hold down the [SHIFT] key and press the [CAL 7] and [CAL SIG LEVEL] keys to set to the CAL LEVEL to −20 dBm.

(6) Hold down the [SHIFT] key and press the [BK SP] key to select the DEBUG mode.
Then, press the following keys in this sequence.
[4] [2] [0] [0] [2] [0] [ENTER] [3] [D] [ENTER]

(7) Adjust R122 so that the △MARKER value enters within ±0.1 dB.

(8) Press the following keys in this sequence.
[4] [2] [0] [0] [2] [0] [ENTER] [3] [F] [ENTER] [4] [2] [0] [0] [2] [2] [ENTER] [1] [ENTER]

(9) Adjust R144 in the same way as for Step (7).

(10) Press the following keys in this sequence.
[4] [2] [0] [0] [2] [2] [ENTER] [2] [ENTER] [4] [2] [0] [0] [0] [4] [ENTER] [1] [1] [ENTER]

(11) Adjust R338 in the same way as for Step (7)

(12) Press the following keys in this sequence.
[4] [2] [0] [0] [0] [4] [ENTER] [1] [ENTER] [RETURN]

(13) Set the CAL LEVEL to −30 dBm.

(14) Hold down the [SHIFT] key and press the [BK SP] key to select the DEBUG mode.

(15) Press the following keys in this sequence.
[4] [2] [0] [0] [2] [0] [ENTER] [3] [B] [ENTER]

(16) Adjust R114 in the same way as for Step (7).

(17) Press the following keys in this sequence.

[4] [2] [0] [0] [2] [0] [ENTER] [3] [7] [ENTER]

(18) Adjust R120 in the same way as for Step (7).

(19) Press the following keys in this sequence.

[4] [2] [0] [0] [2] [0] [ENTER] [2] [F] [ENTER]

(20) Adjust R128 in the same way as for Step (7).

(21) Press the following keys in this sequence.

[4] [2] [0] [0] [2] [0] [ENTER] [1] [F] [ENTER]

(22) Adjust R134 in the same way as for Step (7).

(23) Press the following keys in this sequence.

[4] [2] [0] [0] [2] [0] [ENTER] [3] [F] [ENTER] [RETURN]

5.3.5 28.6 MHz Rejection Circuit Adjustment

- ASSEMBLY ADJUSTMENT
  IF block (WBL-32xxIF)

- RELATED PERFORMANCE TEST
  There is no related performance test.

- DESCRIPTION
  When the interface (IF) frequency of the IF block is converted from 21.4205 MHz to 3.5795 MHz, a +7.159 MHz spurious is generated. The 28.5795 MHz frequency rejection circuit is provided to suppress the spurious generation. The circuit must be adjusted so that the 32.159 MHz spurious is reduced to −100 dBc when the 25 MHz CAL signals are entered in the INPUT terminal of R3265/3271.

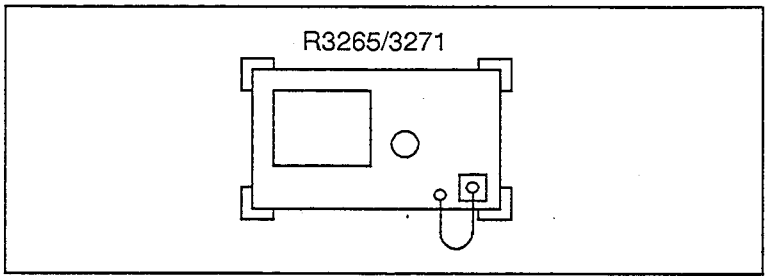


Figure 5-9 28.6 MHz Rejection Circuit Adjustment

- EQUIPMENT

Cable	MC-61; BNC (male), 10 cm long
Adapter	JUG-201A/U; type N (male) to BNC (female)

- PROCEDURE

(1) Turn off the POWER switch of the R3265/3271, unplug the power cord, and remove the system cover. Plug the power cord, turn the POWER switch on, and warm up the system 30 minutes or more.

(2) Connect the BNC cable (using the N-BNC conversion adapter) between the CAL OUT and INPUT terminals of the R3265/3271.

(3) Press the [RESET] key of the R3265/3271, and set the controls as follows:

CENTER FREQ	25 MHz
SPAN	500 Hz
REF. LEVEL	0 dBm
RBW	30 kHz
DIGITAL IF	OFF

(4) Press the [RESET], [MKR→] and [MKR→REF] keys in this sequence on the R3265/3271.

(5) Set the [CENTER FREQ] of the R3265/3271 to 32.159 MHz.
Then, reduce the [PEF LEVEL] 50 dB below the current setup.

(6) Press the [CPL] and [ATT] keys of R3265/3271 to set the Input Attenuator to 0 dB.

(7) Adjust C5 to have the minimum signal level on the screen.

(8) Adjust C6 in the same way as for Step (7).

(9) Adjust C400 in the same way as for Step (7).

(10) Repeat Steps (7) to (9) until the signal level drops below the center scale position of the screen.

5.3.6 YTO Adjustment

- ASSEMBLY ADJUSTMENT
  RF I/O assembly (BLL-017508x01/x02)

- RELATED PERFORMANCE TEST
  Frequency span accuracy

- DESCRIPTION
  Enter the 3.5GHz frequency signals and set the center frequency to 0 Hz. Set the YTO offset of the center frequency to 3.5 GHz, and adjust the YTO gain. The adjustment can be made by changing data of the RF I/O DAC. The first local PLL must be turned off.

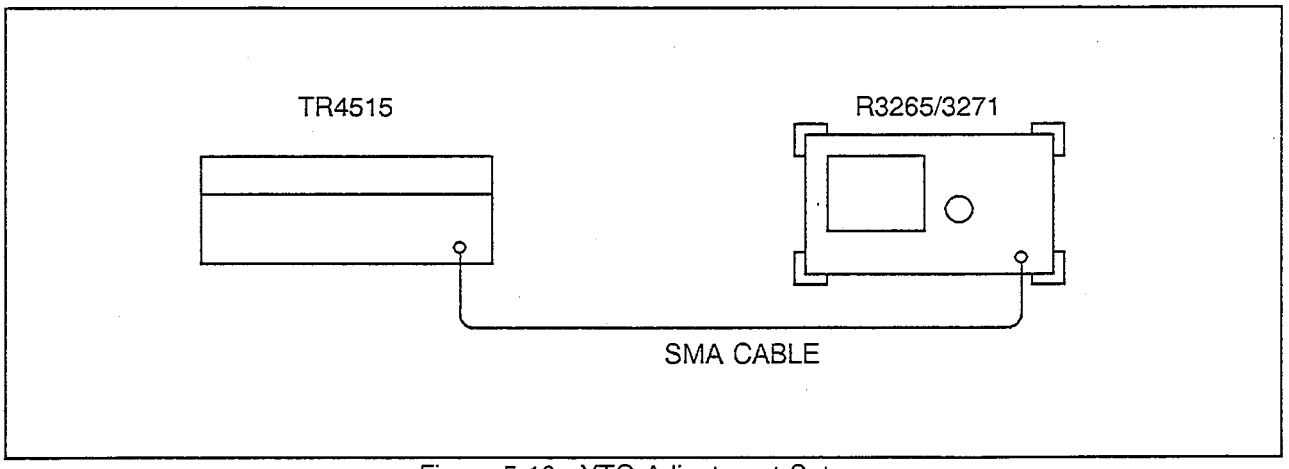


Figure 5-10 YTO Adjustment Setup

- EQUIPMENT

Synthesized sweeper	TR4515
Cable	A01002; SMA (male), 70 cm long

- PROCEDURE

(1) Connect the equipment as illustrated in Figure 5-10.

(2) Press the [INSTR PRESET] key on the TR4515 and set the controls as follows:

CW	3.5 GHz
LEVEL	−20 dBm

(3) Press the [RESET] key on the R3265/3271 and set the controls as follows:

CENTER FREQ ..... 0 Hz
SPAN ..... 100 MHz

(4) Hold down the [SHIFT] key and press the [5] key on the R3265/3271. When the "Please input password!!" message appears, press keys [9], [4], [2], [8] and [4] in this sequence.

(5) Press the [YTO TUNE] and [PLL ON/OFF] keys.

(6) Press the [0 MHZ ADJ] key and adjust the data knob so that the local-feed-through locates within the center scale position ±0.5 div.

(7) Press the [CENTER], [3], [.], [5] and [GHz] keys in this sequence.

(8) Press the [3.5 MHZ ADJ] key and adjust the data knob so that the signal locates within the center scale position ±0.5 div.

(9) Press the [SPAN], [1], [0] and [MHz] keys in this sequence.

(10) Press the [3.5 MHZ ADJ] key and adjust the data knob so that the signal locates within the center scale position ±0.5 div.

(11) Press the [CENTER], [0] and [MHz] keys in this sequence.

(12) Press the [0 MHZ ADJ] key and adjust the data knob so that the local-feed-through locates within the center scale position ±0.5 div.

(13) Repeat Steps (10) to (12) so that the 0 MHz and 3.5GHz signals locate within the center scale position ±1 div.

[Data Writing in EEPROM]

(14) Hold down the [SHIFT] key and press the MARKER [ON] key on the R3265/3271, and wait for approximately 10 seconds. Data writing in the EEPROM will complete.

(15) Press the [PLL ON/OFF], [RETURN] and [RETURN] keys in this sequence.

5.3.7 YTF Adjustment

- ASSEMBLY ADJUSTMENT
  RF I/O assembly (BLL-017508x01/x02)

- RELATED PERFORMANCE TEST
  Image, multiple and out-of-band response
  Second harmonic distortion
  Frequency response

- DESCRIPTION
  The gain and offset of YTF tuning voltage are set by DACs on the RF I/O assembly. The offset DAC value is optimized at a low frequency and the gain DAC value is optimized at a high frequency of each band.

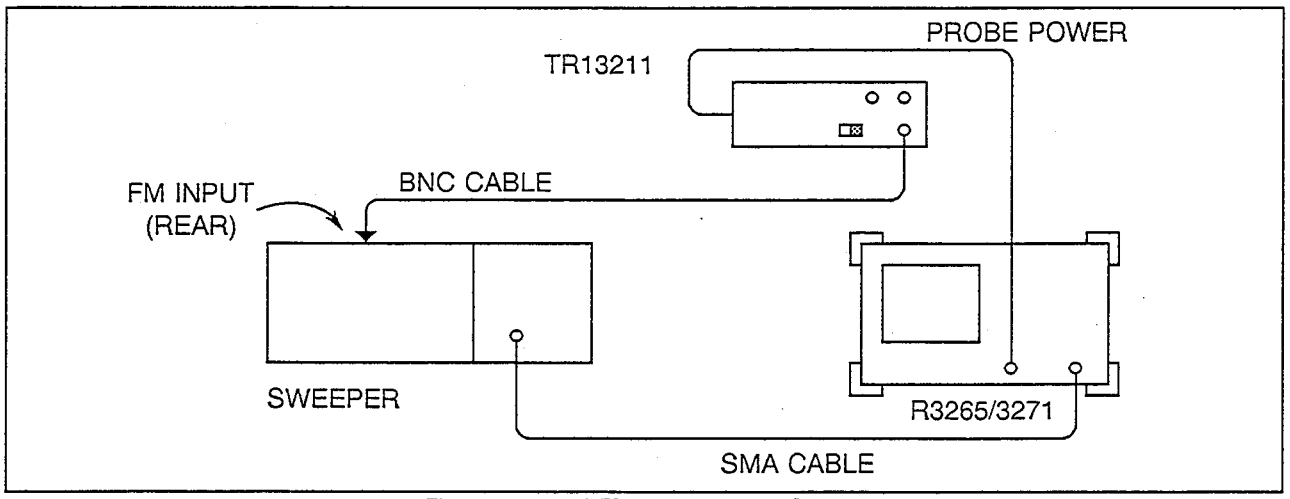


Figure 5-11 YTF Adjustment Setup

- EQUIPMENT

Sweeper:	HP8350 and HP83595A
Sweep adapter:	TR13211
Cable:	A01002; SMA (male), 70 cm long
	MI-09; BNC (male), 150 cm long

- PROCEDURE

(1) Connect the equipment as illustrated in Figure 5-11.

(2) Press the [PRESET] key on the HP8350 and set the controls as follows:

CW	3.7 GHz
Power Level	−2 dBm

(3) Set the TR13211 controls as follows:

FM FREQ	200 Hz
LEVEL	Approx. 10 Vpp
FM SWITCH:	EXT

(4) Press the [PRESET] key on the R3265/3271 and set the controls as follows:

CENTER FREQ	3.7 HGz
RBW:	300 kHz
dB/div:	2 dB/div
SWEEP TIME:	500 msec
SPAN:	0 Hz

(5) Hold down the [SHIFT] key and press the [5] key on the R3265/3271. When the "Please input password!!" message appears, press keys [9], [4], [2], [8] and [4] in this sequence.

(6) Press the [YTF TUNE] and [YTF SWEEP ON/OFF] keys to set YTF SWEEP to "ON".

[3.5 to 7.5GHz Band]

(7) Press the following keys on the R3265/3271:

[BAND SELECT] [2] [Hz] [SPAN] [0] [Hz]

(8) Press the [CENTER] [3] [.] [7] and [GHz] keys in this sequence.

(9) Set the [CW] to 3.7 GHz on the sweeper.

(10) Press the [YTF OFFSET] key on the R3265/3271, and adjust the data control so that the peak of band-pass filter waveforms locates within the center scale position ±0.5 div on the screen.

(11) Set the [CW] to 7.4 GHz on the sweeper.

(12) Press the [CENTER] [7] [.] [4] and [GHz] keys on the R3265/3271.

(13) Press the [YTF GAIN] key on the R3265/3271, and adjust the data control so that the peak of band-pass filter waveforms locates within the center scale position ±0.5 div on the screen.

(14) Repeat Steps (8) to (13) so that the YTF OFFSET and YTF GAIN reach within the center scale position = ±0.5 div.

Caution: Skip Steps (15) to (22) for the R3271. Jump to Step (23).

[7.4 to 8GHz band (R3265 only)]

(15) Press the following keys on the R3265 in this sequence.

[BAND SELECT] [3] [Hz] , [SPAN] [0] [Hz] .

(16) Press the [CENTER] , [7] . [6] and [GHz] keys in this sequence.

(17) Set the [CW] to 7.6 GHz on the sweeper.

(18) Press the [YTF OFFSET] key on the R3265, and adjust the data control so that the peak of band-pass filter waveforms locates within the center scale position ±0.5 div.

(19) Press the [CENTER] , [8] . [3] and [GHz] keys on the R3265 in this sequence.

(20) Set the [CW] to 8.3 GHz on the sweeper.

(21) Press the [YTF GAIN] key on the R3265, and adjust the data control so that the peak of band-pass filter waveforms locates within the center scale position ±0.5 div.

(22) Repeat Steps (16) to (21) so that both the YTF OFFSET and YTF GAIN locate within the center scale position ±0.5 div.

Caution: Skip Steps (23) to (46) for the R3265. Jump to Step (47).

[7.4 to 15.4GHz band (R3271 only)]

(23) Press the following keys on the R3271 in this sequence.

[BAND SELECT] [3] [Hz] , [SPAN] [0] [Hz] .

(24) Press the [CENTER] , [8] . [3] and [GHz] keys in this sequence.

(25) Set the [CW] to 7.6 GHz on the sweeper.

(26) Press the [YTF OFFSET] key on the R3271, and adjust the data control so that the peak of band-pass filter waveforms locates within the center scale position ±0.5 div.

(27) Press the [CENTER], [1], [5] and [GHz] keys on the R3271 in this sequence.

(28) Set the [CW] to 15 GHz on the sweeper.

(29) Press the [YTF GAIN] key on the R3271, and adjust the data control so that the peak of band-pass filter waveforms locates within the center scale position ±0.5 div.

(30) Repeat Steps (24) to (29) so that both the YTF OFFSET and YTF GAIN locate within the center scale position ±0.5 div.

[15.2 to 23.3GHz band (R3271 only)]

(31) Press the following keys on the R3271 in this sequence.

[BAND SELECT] [4] [Hz], [SPAN] [0] [Hz].

(32) Press the [CENTER], [1], [6] and [GHz] keys in this sequence.

(33) Set the [CW] to 16 GHz on the sweeper.

(34) Press the [YTF OFFSET] key on the R3271, and adjust the data control so that the peak of band-pass filter waveforms locates within the center scale position ±0.5 div.

(35) Press the [CENTER], [2], [3] and [GHz] keys on the R3271 in this sequence.

(36) Set the [CW] to 23 GHz on the sweeper.

(37) Press the [YTF GAIN] key on the R3271, and adjust the data control so that the peak of band-pass filter waveforms locates within the center scale position ±0.5 div.

(38) Repeat Steps (32) to (37) so that both the YTF OFFSET and YTF GAIN locate within the center scale position ±0.5 div.

[23 to 26.5GHz band (R3271 only)]

(39) Press the following keys on the R3271 in this sequence.

[BAND SELECT] [5] [Hz], [SPAN] [0] [Hz].

(40) Press the [CENTER], [2], [4] and [GHz] keys in this sequence.

(41) Set the [CW] to 24 GHz on the sweeper.

(42) Press the [YTF OFFSET] key on the R3271, and adjust the data control so that the peak of band-pass filter waveforms locates within the center scale position ±0.5 div.

(43) Press the [CENTER], [2], [6] and [GHz] keys on the R3271 in this sequence.

(44) Set the [CW] to 26 GHz on the sweeper.

(45) Press the [YTF GAIN] key on the R3271, and adjust the data control so that the peak of band-pass filter waveforms locates within the center scale position ±0.5 div.

(46) Repeat Steps (40) to (45) so that both the YTF OFFSET and YTF GAIN locate within the center scale position ±0.5 div.

[Data Writing in EEPROM]

(47) Hold down the [SHIFT] key and press the MARKER [ON] key on the R3265/3271, and wait for approximately 10 seconds. Data writing in the EEPROM will complete.

(48) Press the [YTF SWEEP ON/OFF], [RETURN] and [RETURN] keys in this sequence.

5.3.8 Frequency Response Adjustment

- ASSEMBLY ADJUSTED
  RF I/O assembly (BLL-017508x01/x02)

- RELATED PERFORMANCE TEST
  Frequency response
  Displayed average noise level

- DESCRIPTION
  Enter the RF signals synchronized with the R3265/3271 sweep signals from the sweeper using the sweep adapter.
  Adjust the BAND GAIN and SLOPE GAIN of each band, and adjust the MIXER BIAS for the R3271 band greater than 3.5 GHz. Before the frequency response adjustment, the YTF adjustment has been completed.

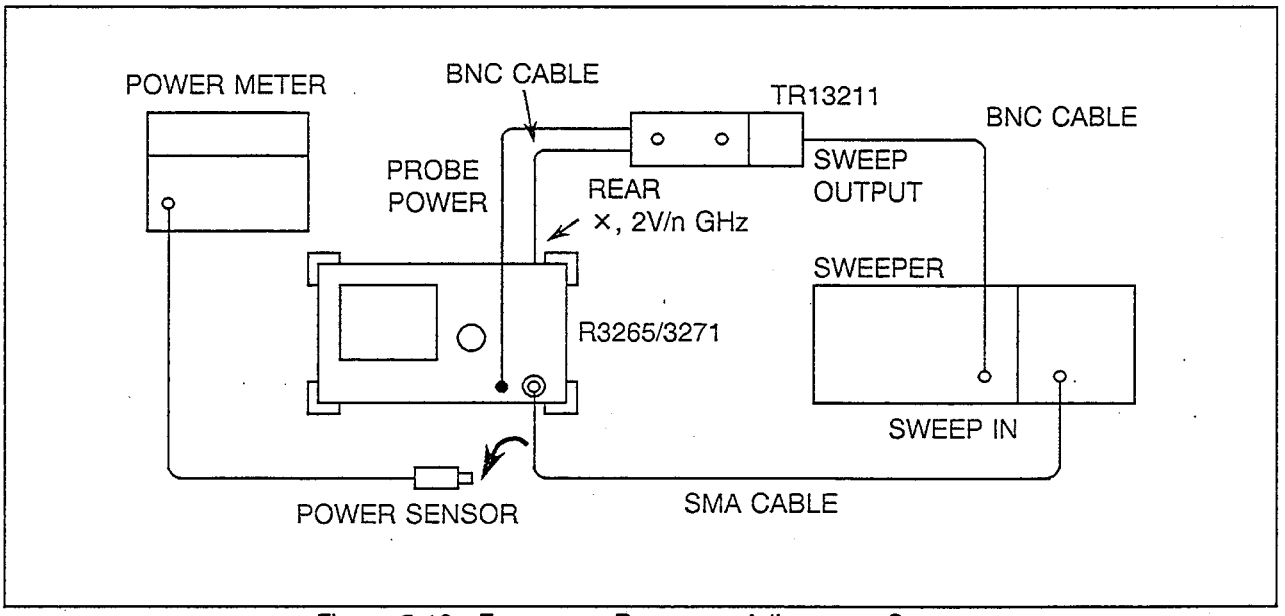


Figure 5-12 Frequency Response Adjustment Setup

- EQUIPMENT

Sweeper:	HP8350 and HP83595A
Sweep adapter:	TR13211
Power meter:	HP436A
Power sensor:	HP8485A
Cable:	
A01002;	SMA (male), 70 cm long
Two MI-09's;	BNC (male), 150 cm long

- PROCEDURE

(1) Zero and calibrate the power meter. Rotate and set the CAL FACTOR control to the 2GHz calibration factor of the power sensor.

(2) Connect the equipment as illustrated in Figure 5-12.

(3) Press the [INSTR PRESET] key on the HP8350, and set the control as follows:

START FREQ:	10 MHz
STOP FREQ:	3.6 GHz
POWER LEVEL:	−4 dBm
SWEEP:	EXT
SWEEP TRIGGER:	EXT

(4) Press the [PRESET] key on the R3265/3271, and set the controls as follows:

START:	0 MHz
STOP:	3.6 GHz
SWEEP TIME:	500 msec

(5) Set the controls of TR13211 as follows:

FM:	INT
FREQ:	100 Hz
LEVEL:	Center position of variable range

(6) Press the [START] key on the TR13211, and adjust the START control so that the signal overlaps on the left vertical axis of the screen on the R3265/3271.

(7) Press the [STOP] key on the TR13211, and adjust the STOP control so that the signal overlaps on the right vertical axis of the screen on the R3265/3271.

(8) Press the [SWEEP] key on the TR13211, and fine adjust the START and STOP controls of the TR13211 so that the signals are displayed on the entire R3265/3271 screen from its leftmost end to the rightmost end. (For the TR13211 operations, refer to the TR13211 operation manual.)

(9) Disconnect the SMA cable from the input terminal of R3265/3271, and connect the power sensor to it.

(10) Press the [MENU], [SWEEP MODE], and [SINGLE SWP] keys on the R3265/3271, and set the sweep time to 20 seconds.

(11) Press the [MENU], [SWEEP MODE], and [SINGLE SWP] keys on the R3265/3271, and measure the frequency characteristics of sweeper output on the power meter. Using the result data, adjust the POWER LEVEL and SLOPE controls of the sweeper so that the frequency characteristics waveforms enter within −4 dBm ±1 dB.

(12) Press the [MENU], [SWEEP MODE], and [SINGLE SWP] keys on the R3265/3271, and repeat Step (11) until the frequency characteristics waveforms enter within −4 dBm ±1 dB.

(13) Press the [SAVEn] and [1] keys on the sweeper.

(14) Disconnect the SMA cable from the power sensor, and connect it to the R3265/3271 input.

(15) Press the [MENU], [SWEEP MODE], and [CONT SWP] keys on the R3265/3271, and set the controls as follows:

SWEEP TIME:	500 msec
START:	3.61 GHz
STOP:	7.5 GHz

Rotate and adjust the CAL FACTOR control of the power meter to the 6GHz calibration factor of power sensor.

(16) Repeat Steps (6) to (12).

(17) Press the [SAVEn] and [2] keys of the sweeper.

(18) Disconnect the SMA cable from the power sensor, and connect it to the R3265/3271 input.

Caution: Skip Steps (19) to (22) for the R3271. Jump to Step (23).

[R3265 only]

(19) Press the [MENU], [SWEEP MODE], and [CONT SWP] keys on the R3265, and set the controls as follows:

SWEEP TIME:	500 msec
START:	7.5 GHz
STOP:	8.3 GHz

Rotate and adjust the CAL FACTOR control of the power meter to the 6GHz calibration factor of power sensor.

(20) Repeat Steps (6) to (12).

(21) Press the [SAVEn] and [3] keys of the sweeper.

(22) Disconnect the SMA cable from the power sensor, and connect it to the R3265/3271 input.
Skip Steps (23) to (34), and jump to Step (35).

[R3271 only]

(23) Press the [MENU], [SWEEP MODE], and [CONT SWP] keys on the R3271, and set the controls as follows:

SWEEP TIME:	500 msec
START:	7.5 GHz
STOP:	15.4 GHz

Rotate and adjust the CAL FACTOR control of the power meter to the 12GHz calibration factor of power sensor.

(24) Repeat Steps (6) to (12).

(25) Press the [SAVEn] and [3] keys of the sweeper.

(26) Disconnect the SMA cable from the power sensor, and connect it to the R3271 input.

(27) Press the [MENU], [SWEEP MODE], and [CONT SWP] keys on the R3271, and set the controls as follows:

SWEEP TIME: ..... 500 msec
START: ..... 15.4 GHz
STOP: ..... 23.3 GHz

Rotate and adjust the CAL FACTOR control of the power meter to the 20GHz calibration factor of power sensor.

(28) Repeat Steps (6) to (12).

(29) Press the [SAVEn] and [4] keys of the sweeper.

(30) Disconnect the SMA cable from the power sensor, and connect it to the R3271 input.

(31) Press the [MENU], [SWEEP MODE], and [CONT SWP] keys on the R3271, and set the controls as follows:

SWEEP TIME: ..... 500 msec
START: ..... 23.3 GHz
STOP: ..... 26.5 GHz

Rotate and adjust the CAL FACTOR control of the power meter to the 25GHz calibration factor of power sensor.

(32) Repeat Steps (6) to (12).

(33) Press the [SAVEn] and [5] keys of the sweeper.

(34) Disconnect the cable from the power sensor, and connect it to the R3271 input.

[R3265/3271]

(35) Press the [MENU], [SWEEP TIME], and [CONT SWEEP] keys on the R3265/3271, and set the controls as follows:

START: ..... 10 MHz
STOP: ..... 3.6 GHz
SWEEP TIME: ..... 500 msec
dB/div: ..... 2 dB/div
DISP LINE ..... −4 dBm

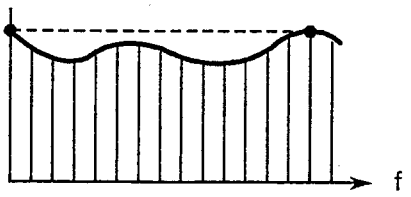
(36) Hold down the [SHIFT] key and press the [5] key on the R3265/3271. When the "Please input password!!" message appears, enter "94284" for the password. Then, press the [MIX TUNE] key.

(37) Press the [BAND SELECT], [1] and [Hz] keys in this sequence on the R3265/3271.

(38) Press the [RECALLn] and [1] keys on the sweeper.

(39) Fine adjust the START and STOP controls of the TR13211 so that the signals continue from the leftmost end to the rightmost end of the R3265/3271 screen.

(40) Press the [SLOPE GAIN] key on the R3265/3271, and adjust the data control so that the peak of lower band of frequency characteristics waveforms almost matches the peak of the higher hand. If the peak level has reached the end of variable range, use this position.



(41) Press the [BAND GAIN] key on the R3265/3271, and adjust the data control so that the peak of frequency characteristics waveforms locates within the range of 0 to -1 dB from the DISP LINE.

(42) Press the following keys in this sequence.

[BAND SELECT] [2] [Hz] [START] [3] [.] [6] [1] [GHz]

(43) Press the [RECALLn] and [2] key s on the sweeper.

(44) Repeat Steps (39) to (41).

[R3271 only]

(45) Press the [BIAS ADJ FIX/NAR] key on the R3271, and adjust the data control so that the entire frequency characteristics curve reaches its peak level.

Caution: Skip Steps (46) to (48) for the R3271, and jump to Step (50).

[R3265 only]

(46) Press the following keys in this sequence on the R3265.

[BAND SELECT] [3] [Hz] [START] [7] [.] [5] [GHz] [STOP] [8] [.] [3] [GHz]

(47) Press the [RECALLn] and [3] keys on the sweeper.

(48) Repeat Steps (39) to (41).

(49) Jump to Step (62) for data writing in the EEPROM.

[R3271 only]

(50) Press the following keys in this sequence on the R3271.

[BAND SELECT] [3] [Hz] [START] [7] [.] [5] [GHz]

(51) Press the [RECALLn] and [3] keys on the sweeper.

(52) Repeat Steps (39) to (41).

(53) Press the [BIAS ADJ FIX/NAR] key on the R3271, and adjust the data control so that the entire frequency characteristics curve reaches its peak level. If the frequency characteristics change, repeat Steps (40) and (41).

(54) Press the following keys in this sequence on the R3271.

[BAND SELECT] [4] [Hz] [START] [1] [5] [.] [4] [GHz]

(55) Press the [RECALLn] and [4] keys on the sweeper.

(56) Repeat Steps (39) to (41).

(57) Press the [BIAS ADJ FIX/NAR] key on the R3271, and adjust the data control so that the entire frequency characteristics curve reaches its peak level. If the frequency characteristics change, repeat Steps (40) and (41).

(58) Press the following keys in this sequence on the R3271.

[BAND SELECT] [5] [Hz] [START] [2] [3] [.] [3] [GHz] [STOP] [2] [6] [.] [5] [GHz]

(59) Press the [RECALLn] and [5] keys on the sweeper.

(60) Repeat Steps (39) to (41).

(61) Press the [BIAS ADJ FIX/NAR] key on the R3271, and adjust the data control so that the entire frequency characteristics curve reaches its peak level. If the frequency characteristics change, repeat Steps (40) and (41).

[Data writing in the EEPROM]

Caution: The original data is all erased from the EEPROM when data is written in it.

(62) Hold down the SHIFT key and press the ON key on the R3265/3271, and wait for approximately 10 seconds. The data will be written in the EEPROM.

(63) Press the RETURN key twice.

5.3.9 Calibrator Amplitude Adjustment

- ASSEMBLY ADJUSTED
  WBL-32xxSYN (Synthesizer block)

- RELATED PERFORMANCE TEST
  Calibration amplitude accuracy

- DESCRIPTION
  The CALOUT amplitude is adjusted for −10.00 dBm measured directly at the front panel CALOUT jack.

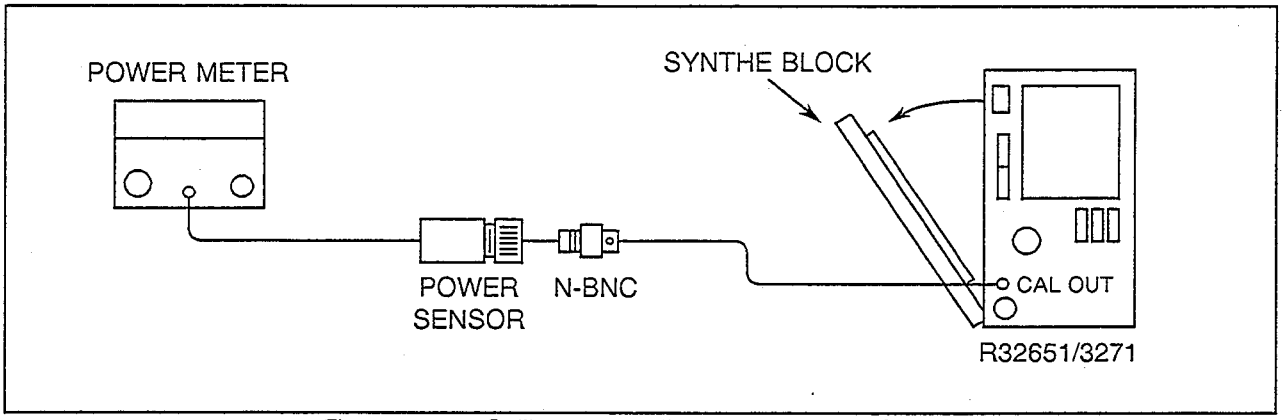


Figure 5-13 Calibrator Amplitude Adjustment Setup

- EQUIPMENT
  Power meter: HP436A
  Power sensor: HP8481A
  Adapter
  Type N (female) to BNC (male): . . . . . NJ-BNCP

- PROCEDURE

(1) Turn off the POWER switch of the R3265/3271, and disconnect the power cord. Remove the analyzer cover, place the analyzer as shown in Figure 5-13, and fold down the SYNTHE BLOCK assembly.

(2) Turn on the POWER switch of R3265/3271, and warm it up at least 30 minutes before starting adjustment.

(3) Zero and calibrate the power meter in the Log Display mode. Enter the 25MHz CAL FACTOR signal of the power sensor to the power meter.

(4) Connect the R3265/3271 through an N-BNC adapter directly to the CALOUT jack on the R3265/3271 front panel.

(5) Adjust R151 of the SYNTHE block for a −10.00 dBm reading on the power meter display.

5.3.10 10MHz Frequency Reference Adjustment

- ASSEMBLY ADJUSTED
  Frequency reference assembly (WBL-32xxSTD)

- RELATED PERFORMANCE TEST
  Frequency readout accuracy and frequency counter marker accuracy
  Frequency reference output accuracy

- DESCRIPTION
  Connect the signal cable between the 10MHz terminal of the Frequency Standard unit and the Frequency Comparator unit. Also, connect the cable between the 10MHz REF OUT terminal at the rear panel of R3265/3271 and the Frequency Comparator unit. Adjust the internal crystal oscillator of the R3265/3271.

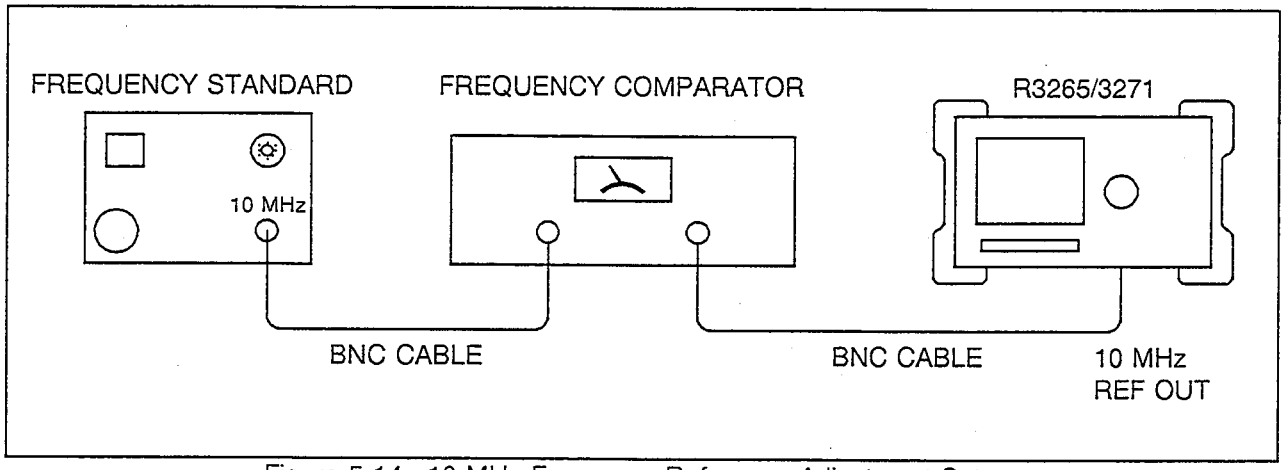


Figure 5-14 10 MHz Frequency Reference Adjustment Setup

- EQUIPMENT
  Frequency Standard unit: TR3110
  Frequency comparator (supporting 10MHz, 1x10 -9 signal detection)
  Cables:
  Two MI-09 cables with BNC (male), 150 cm long

- PROCEDURE

NOTE

Allow the R3265/3271 warm up for at least 30 minutes before performing this adjustment.

(1) Connect the equipment as shown in Figure 5-14.

(2) Set the 10MHz REF of the R3265/3271 to INT.

Press the [CENTER FREQ] and set the [10MHz REF INT/EXT] to INT.

NOTE

When the 10MHz reference is set to EXT, the crystal oscillator is not operating nor warmed up. If the reference is set to EXT, set the reference to INT and allow 30 minutes for the crystal oscillator warm up.

(3) Hold down the [SHIFT] key and press the [CAL 7] key to select the [CAL FREQ REF]. Then, adjust the data control so that the frequency comparator indicates the value within $\pm 1 \times 10^{-8}$.

(4) Press the [Hz] key to store the adjusted data.

NOTE

If the adjusted data is within ±100 but if it cannot be adjusted, set the data to zero and directly adjust the 10MHz reference crystal oscillator as follows.

(5) Adjust the data control to set the data to zero, and press the [Hz] key to store the data.

(6) Turn off the [POWER] switch of the R3265/3271, and disconnect the power cord and signal cables. Remove the analyzer cover, and fold down the WBL-32xxSYN synthesizer block.

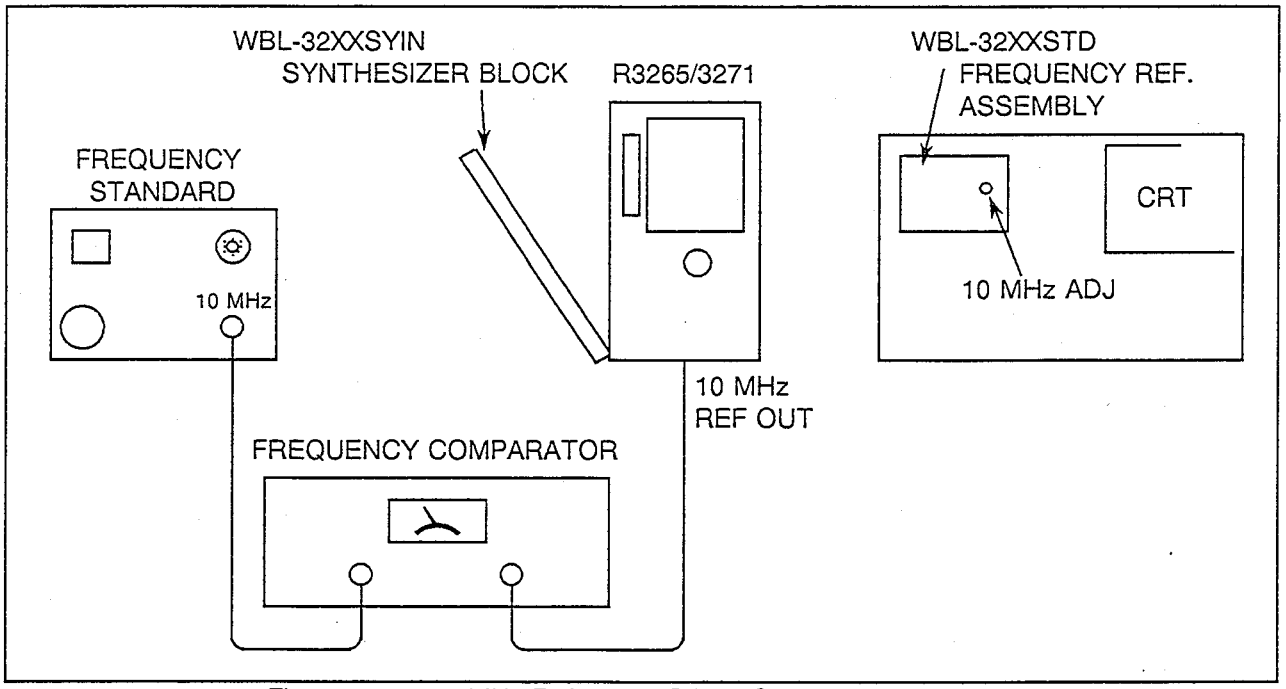


Figure 5-15 10 MHz Reference Cristal Oscillator Adjustment

(7) Connect the equipment as shown in Figure 5-15.

(8) Adjust the 10MHz ADJ control of the WBL-32xxSTD unit so that the indicator of frequency comparator reaches within $\pm 1 \times 10^{-8}$.

NOTE

Allow the R3265/3271 warmup for at least 30 minutes before performing this adjustment.

5.3.11 Frequency Span Adjustment

- ASSEMBLY ADJUSTED
  WBL-3265 I/O
  WBL-3271 I/O

- RELATED PERFORMANCE TEST
  Frequency span accuracy

- DESCRIPTION
  Adjust the frequency span to have an appropriate Span Adjust DAC value of the WBL-3265 I/O (or WBL-3271 I/O).

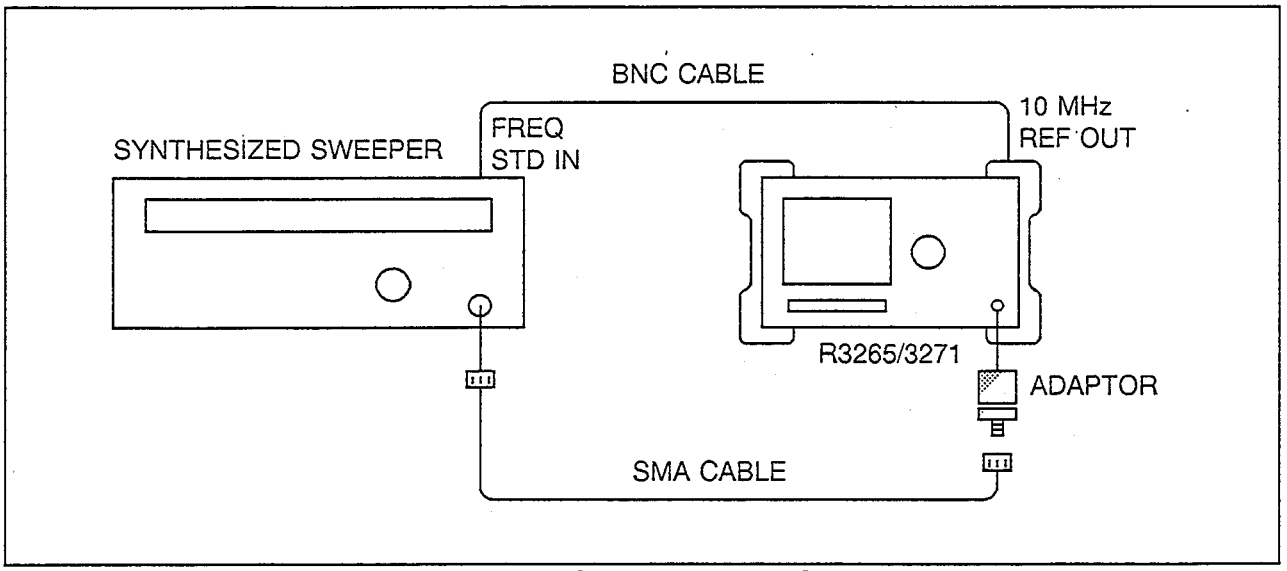


Figure 5-16 SPAN Adjustment Setup

- EQUIPMENT

Synthesized sweeper:	TR4515
Adapter:	
HTM-554S;	Type N (male) to SMA (female)
Cables:	
A01002;	SMA (male), 70 cm long
MI-09;	BNC (male), 150 cm long

- PROCEDURE

(1) Connect the equipment as shown in Figure 5-16.

(2) Set the TR4515 controls as follows:

CW: ..... 3.25 GHz
OUTPUT POWER: ..... −20 dBm

(3) Press the [PRESET] key on the R3265/3271, and set the controls as follows:

START FREQ: ..... 100 MHz
STOP FREQ: ..... 3.6 GHz
REF LEVEL: ..... −10 dBm

(4) Press the [PEAK] and [NEXT MENU] keys to set the [CONT PK ON/OFF] to ON.

(5) Hold down the [SHIFT] key and press the [5] key, enter "94284" for password, and select the MAINTENANCE mode.

(6) Hold down the [SHIFT] key and press the [SPAN] key, and the following software menu will appear on the CRT screen.

LIN		CENTER
LOG	START	SPAN
	STOP	START
	LOG GAIN	STOP
	LOG OFFSET	SPAN ADJ
	RETURN	RETURN

NOTE

Once the MAINTENANCE mode is selected, each function can be set by software keys only.

(7) Press the [LIN] and [SPAN ADJ] keys, and adjust the data control to have the marker indication of 3.250 GHz ±10 MHz.

(8) Set the SYNTHESIZER SWEEPER frequency and the [START] and [STOP] frequencies of the R3265/3271 as defined on Table 5-3. Adjust the [SPAN ADJ] control to have the marker frequency within the limit given on the table.

(9) Hold down the [SHIFT] key and press the MARKER [ON] key to write the adjusted data in the EEPROM.

Table 5-3 Span Adjustment

TR4515 Frequency	R3265/3271		Marker Indication	
	START Frequency	STOP Frequency	MIN	MAX
3.25 GHz	100 MHz	3.6 GHz	3.240 GHz	3.260 GHz
7.3 GHz	100 MHz	8.1 GHz	7.280 GHz	7.320 GHz
460 MHz	100 MHz	500 MHz	458 MHz	462 MHz
136 MHz	100 MHz	140 MHz	135.8 MHz	136.2 MHz
109 MHz	100 MHz	110 MHz	108.95 MHz	109.05 MHz
101.8 MHz	100 MHz	102 MHz	101.79 MHz	101.81 MHz
100.36 MHz	100 MHz	100.4 MHz	100.358 MHz	100.362 MHz
100.018 MHz	100 MHz	100.02 MHz	100.0179 MHz	100.0181 MHz

[LOG SPAN Adjustment]

(10) Press the [RETURN] and [LOG] keys.

(11) Press the following keys in this sequence.

[START] [1] [MHz] [STOP] [1] [GHz]

(12) Set the synthesized sweeper frequency to 10 MHz.

(13) Press the [LOG OFFSET] key and adjust the data control to have the marker frequency of 10 ±0.1 MHz.

(14) Set the synthesized sweeper frequency to 900 MHz.

(15) Press the [LOG GAIN] key and adjust the data control to have the marker frequency of 900 ±10 MHz.

(16) Repeat Steps (12) to (15), and adjust the data control so that the marker frequency comes within the limit defined on Table 5-4.

(17) Set the synthesized sweeper frequency and the [START] and [STOP] frequencies of R3265/3271 to the values defined on Table 5-4, and repeat Steps (12) to (15).

(18) Hold down the [SHIFT] key and press the [ON] key to write the adjusted data in the EEPROM.

Table 5-4 LOG SPAN Adjustment

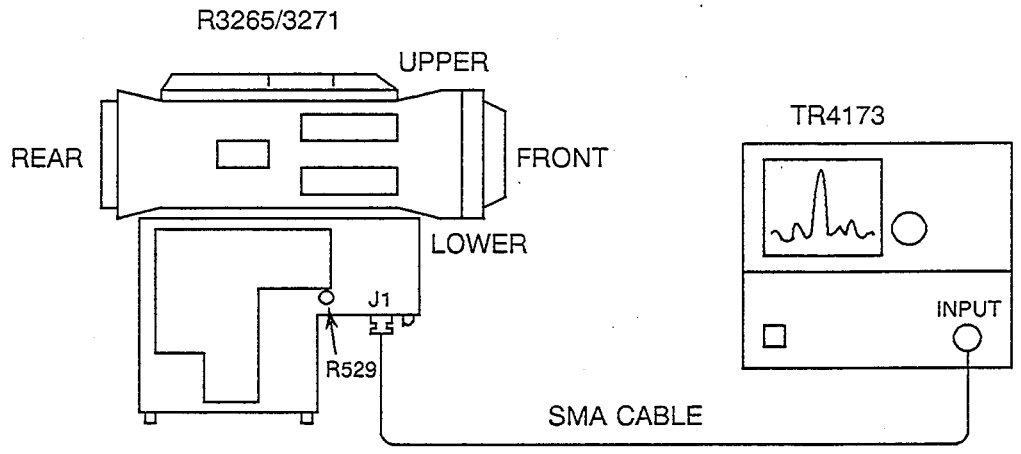
R3265/3271			TR4515 Frequency	Marker Indication	
START FREQ.	STOP FREQ.	Adjustment.		MIN	MAX
1 MHz	1 GHz	LOG OFFSET	10 MHz	9.9 MHz	10.1 MHz
		LOG GAIN	900 MHz	890 MHz	910 MHz
10 MHz	1 GHz	LOG OFFSET	20 MHz	19.8 MHz	20.2 MHz
		LOG GAIN	900 MHz	890 MHz	910 MHz
100 MHz	1 GHz	LOG OFFSET	200 MHz	198 MHz	202 MHz
		LOG GAIN	900 MHz	890 MHz	910 MHz

5.3.12 Sample Synthesizer Adjustment

- ASSEMBLY ADJUSTED
  Synthesizer block (WBL-32xxSYN)

- RELATED PERFORMANCE TEST
  There is no related performance test.

- DESCRIPTION
  The doubler of the sample synthesizer must be adjusted using the variable resistor to suppress spurious.



Note) The R529 adjusting hole is covered with the aluminum tape. Remove the tape and adjust the R529.

Figure 5-17 Sampler Synthe Adjustment

- EQUIPMENT
  Spectrum analyzer: TR4173
  Cable:
  A01002; . . . . . SMA (male), 70 cm long

- PROCEDURE

(1) Remove the cover from the system.

(2) Remove three screws from the synthesizer board.

(3) Unplug the SMA connector from J1.

(4) Connect the SMA cable between J1 and TR4173 (see Figure 5-17).

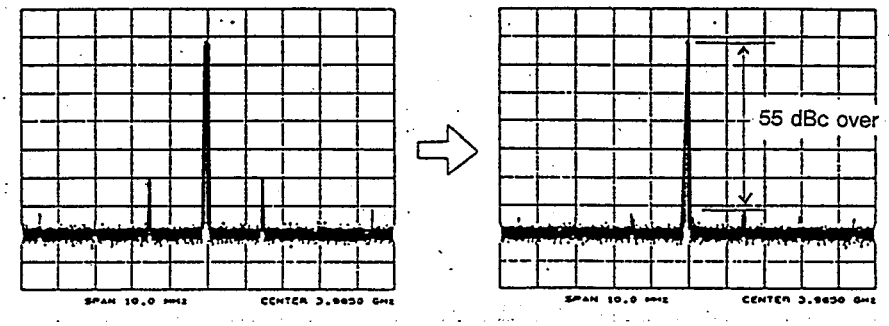
(5) Turn on the POWER switch of R3265/3271, and set the controls as follows:

CENTER FREQ:	40 MHz
SPAN:	10 MHz

(6) Set the TR4173 controls as follows:

CF:	3985 MHz
SPAN:	10 MHz
REF:	−20 dBm
RBW:	10 kHz
VBW:	300 kHz

(7) Make sure that the carrier exists at the center of TR7143 waveforms, and adjust the R529 so that the side signal amplitude is 55 dBc or more.



(8) Unplug the SMA cable from J1, and plug the original cable.

5.3.13 EXT Mixer Adjustment

- ASSEMBLY ADJUSTED
  RF I/O assembly (BLL-017508x01/x02)

- RELATED PERFORMANCE TEST
  There is no related performance test.

- DESCRIPTION
  Enter the 421.42MHz signals of the IF frequency of external (EXT) mixer to the first Lo OUT terminal, and adjust the BAND GAIN control of the EXT mixer band.

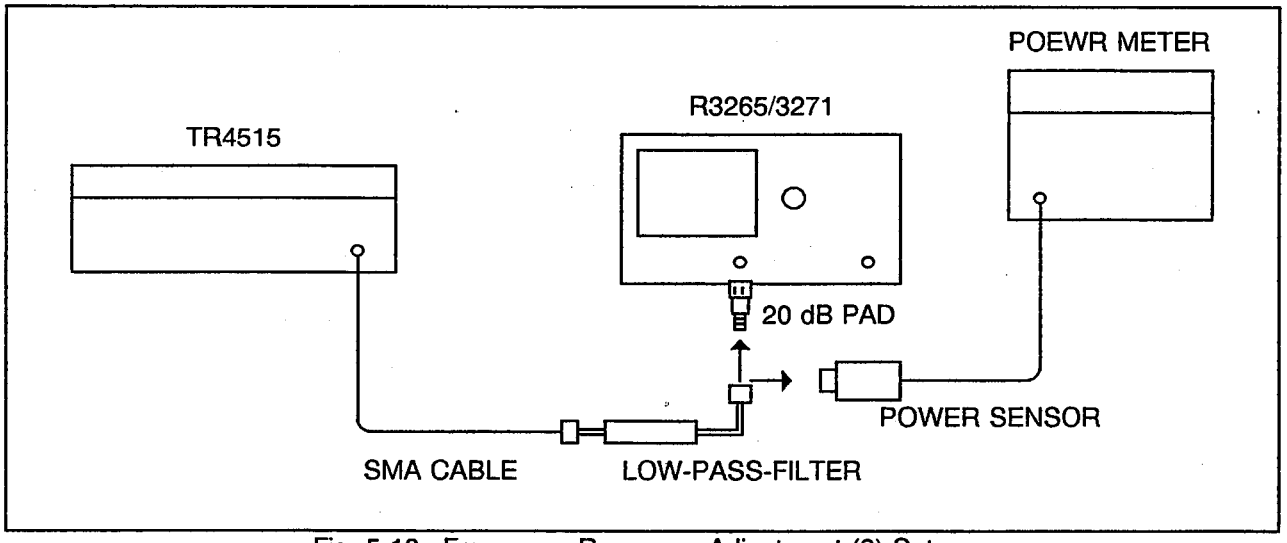


Fig. 5-18 Frequency Response Adjustment (2) Setup

- EQUIPMENT

Synthesized sweeper:	TR4515
Power meter:	HP436A
Power sensor:	HP8485A or HP8481A
2GHz low-pass filter:	DEE-001172-1
20dB PAD:	DEE-000480-1
Adapter:	
HRM-501;	SMA (female) to SMA (female)
Cable:	
A01002;	SMA (male)

- PROCEDURE

(1) Zero and calibrate the power meter. Rotate and adjust the CAL FACTOR control to set the 421MHz calibration factor of the power sensor.

(2) Connect the equipment as illustrated in Figure 5-18. However, connect the low-pass filter output to the power sensor.

(3) Press the [PRESET] key of the TR4515, and set the controls as follows:

CW: ..... 421.42 MHz
POWER LEVEL: ..... −5 dBm

(4) Adjust the POWER LEVEL of the TR4515 so that the power meter indicates −5 dBm.

(5) Connect the low-pass filter output to the 20dB PAD, and connect to the 1st Lo OUT terminal of the R3265/3271.

(6) Press the [PRESET] and [CENTER FREQ] keys on the R3265/3271 to set the [MIX EXT].

(7) Hold down the [SHIFT] key and press the [5] key on the R3265/3271. When the "Please input password!!" message appears, enter "94284" for the password. Then, press the [MIX TUNE] key.

(8) Press the following keys and adjust the DATA control so that the signals appear on a horizontal line on the screen and they reach within ±1 dB from the top of the screen.

[BAND SELECT] [1] [0] [Hz] [SLOPE GAIN] [0] [Hz] [BAND GAIN]

[Data writing in EEPROM]

Caution: The original data is all erased from the EEPROM when data is written in it.

(9) Hold down the [SHIFT] key and press the MARKER [ON] key on the R3265/3271, and wait for approximately 10 seconds. The data will be written in the EEPROM.

(10) Press the [RETURN] key twice.

MEMO

6. TROUBLE SHOOTING

6.1 Repairing Method for Each Board

Table 6-1 List of Repairing Method for Each Board

Board name	Repairing method	Remarks
RF I/O	Replace the part.	Adjustment of relevant parts is needed.
2nd/3rd	Replace the part.	Adjustment of relevant parts is needed.
FRONT END	Replace the part.	Adjustment of relevant parts is needed.
IF	Replace the part.	Adjustment of relevant parts is needed.
LOG, A/D	LOG section: Replace the part. → Adjustment of relevant parts is needed. A/D section : Replace the board. → Whole adjustment of the A/D and LOG sections is needed.	
CPU	Replace the board.	When the board is replaced, whole readjustment is needed.
SYNTHE	Replace the part.	Adjustment of relevant parts is needed.

6.2 Power Supply Section

6.2.1 Lighting of REMOTE Lamp

If the REMOTE lamp does not go on, or if the lamp goes on, but comes off immediately, a power failure may exist. Check the fuse and fan motor operation and check that the rear LED flashes.

If the CRT does not display anything for more than five seconds in spite of continuous lighting of the REMOTE lamp, it is considered that the clock signal is not input to the CPU.

6.2.2 Check of Fuse

Take out the fuse. If it is conducting, the secondary side of the power supply or later may be in failure. Check the fan motor operation and check that the rear LED flashes. If the fuse is melting, the primary side of the power supply may be in failure.

6.2.3 Fan Motor Operation

If the fan motor rotates, the secondary side of the power supply or later may be in failure. Check that the rear LED flashes.

If the fan motor does not rotate, the power supply or fan motor may be in failure. If the fan motor rotates with other + 12 Vdc, the power supply may be in failure.

6.2.4 Flashing of Rear LED

Turn off the power switch and remove the power cable. Remove panel ① shown in Figure 6-1 and remove the output connector from the power supply. Reinstall the power cable and turn on the power switch to check that the rear LED flashes.

If the rear LED does not go on, the power supply may be in failure. If the rear LED goes on, it is considered that any part other than the power supply is short-circuited, activating the overcurrent protection circuit.

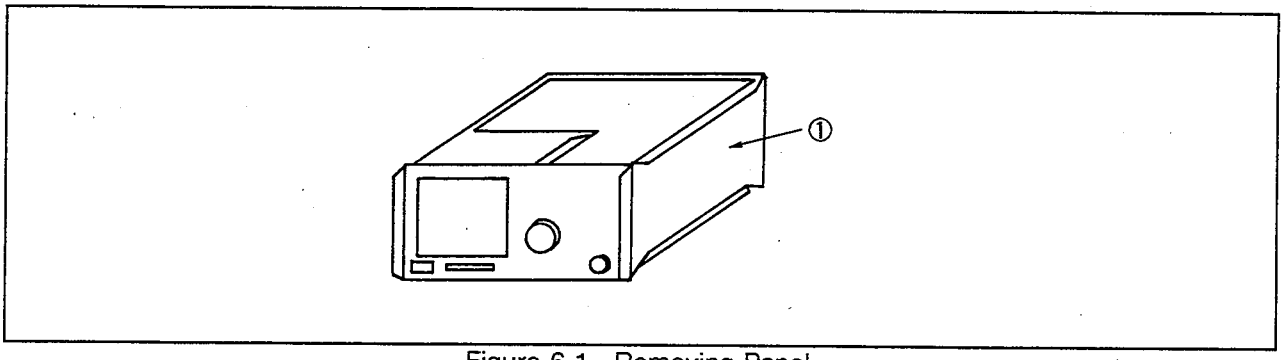


Figure 6-1 Removing Panel

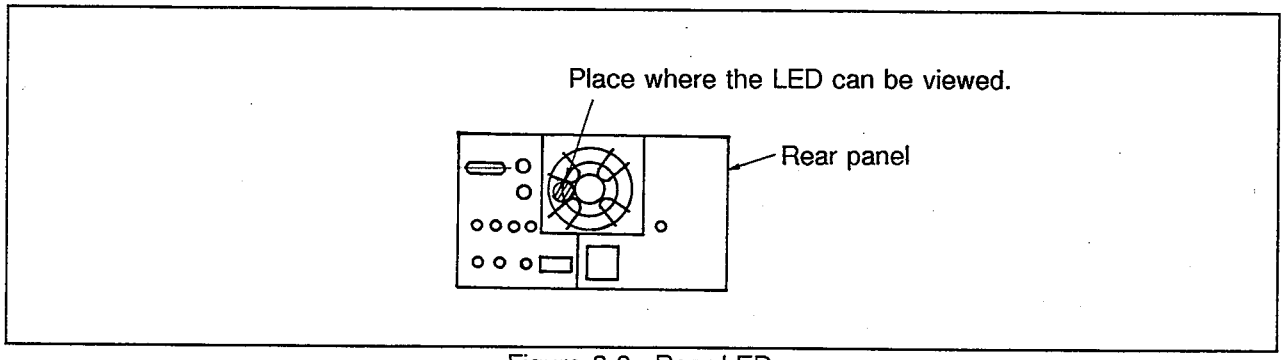


Figure 6-2 Rear LED

6.2.5 Failure of Output Voltage

Remove panel ① shown in Figure 6-1 and remove the output connector from the power supply. Check if specified voltages are output (see Figure 6-3). Table 6-2 shows connector pin Nos. and output voltages.

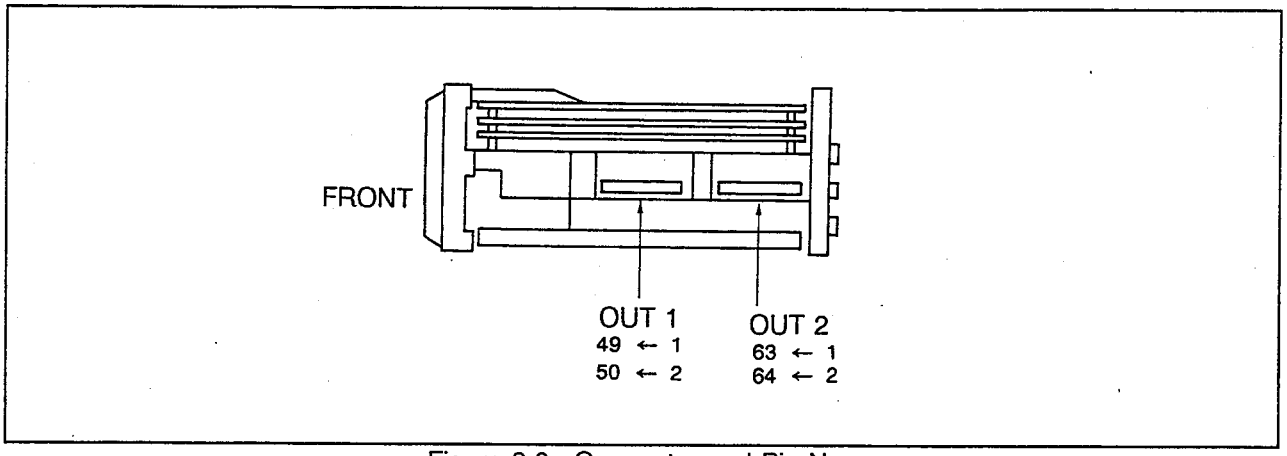


Figure 6-3 Connector and Pin No.

Table 6-2 Connector Pin No.

Connector	Pin No.	Output voltage
OUT 1 (J2)	1, 2, 5, 6, 7, 8, 9, 10	+15V
	15, 16, 19, 20, 21, 22, 25, 26, 27, 28	−15V
	31, 32	+20V
	35, 36	+34V
	39, 40	+24V
	43, 44, 45, 46	+12V
OUT 2 (J1)	41, 42, 45, 46, 47, 48	+5.05V
	53, 54, 55, 56, 57, 58	+5V

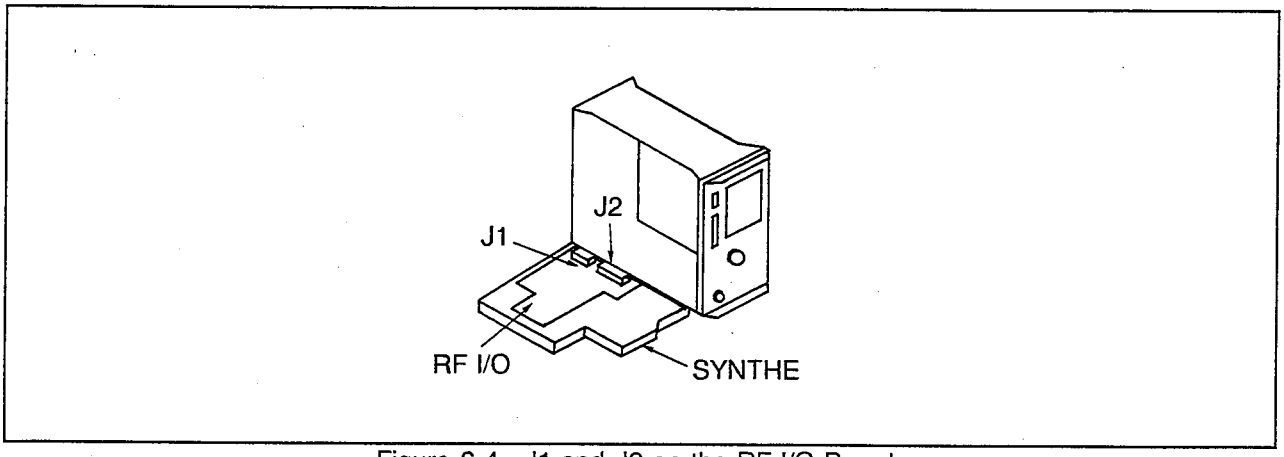


Figure 6-4 J1 and J2 on the RF I/O Board

If the measured voltage is not within ±1% from the output voltage, the power supply may be in failure. If the measured voltage is within ±1% from the output voltage, reinstall the connector and panel to check J1 and J2 on the RF I/O board (see Figure 6-4).

The relation between the power supply and RF I/O board connectors is such that OUT1 corresponds to J2, and OUT2 corresponds to J1. If the measured voltage is not within ±1% from the output voltage, the power supply may be in failure.

6.3 RF Section

6.3.1 1st LO ISO AMP

(1) Connect a DVM's positive lead to +12V pin (C1, C2) and negative lead to the GND pin (case).

(2) The voltage measured on the DVM should be +12 V. Otherwise, The RF I/O may be in failure.

(3) Table 6-3 shows each port gain to the YTO IN port.

Table 6-3 Gain for each Port

Connector	Connector
TO DUAL MIXER	+1 dB (min)
TO 1ST SAMPLER	−27 dB (min)
TO EXT MIXER	−7 dB (min)

Set the span of the R3265/3271 to zero, measure the YTO output power with a power meter, then connect to the YTO IN in the 1st LO ISO AMP. Measure the output power of each port to calculate the gain. If the gain is low, replace the 1st LO ISO AMP.

(4) The DC voltage applied to the bias terminal (C3) is output to the J4 (TO EXT MIXER) port (1st LO OUT on the front panel).

Press [CENTER FREQ], [MIX EXT] and [POSI BIAS] or [NEGA BIAS] on the R3265/3271.

Turn the data knob and measure the J4 on the DVM to check that the DC voltage value changes.
If no voltage is output to the bias terminal, the RF I/O may be in failure.
If the voltage is output to the bias terminal and the same voltage is not output to J4, the 1st LO ISO AMP may be in failure.

6.3.2 Dual Band Mixer

[Band SW]

(1) Connect a DVM's passive lead to band SW terminal (C1) and negative lead to the case.

(2) The voltage value measured on the DVM depends on the band as shown in Table 6-4.

Table 6-4 The Voltage Measured (Band SW)

CENTER FREQ	Voltage
1 GHz	−3.8V to −1.8V
4 GHz	+0.8V to +2.8V

Set the span of the R3265/3271 to zero and measure the band SW terminal voltage for each of 1 GHz and 4 GHz CENTER FREQ setting.

(3) If the voltage is out of the range shown in Table 6-4, remove the connector from J13 on the RF/I/O board, measure pin 4 of J13 on the DVM, then set the CENTER FREQ of the R3265/3271 to check that the voltage is output as shown below.

CENTER FREQ 1 GHz ..... +14 to +15V

CENTER FREQ 4 GHz ..... −14 to −15V

If the voltage is out of the range, the RF I/O board may be in failure.

[Mixer Bias]

No mixer bias exists in the R3265.

(1) Connect a DVM's passive lead to bias terminal (C2) and negative lead to the case.

(2) The voltage measured on the DVM depends on the band as shown in Table 6-5.

Table 6-5 The Voltage Measured (mixer bias: R3271 only)

CENTER FREQ	Voltage
5 GHz	+1V to +3V
10 GHz	0V to +1.7V
20 GHz	+2.3V to +4.3V
25 GHz	+0.1 to +2.1V

Set the span of the R3265/3271 to zero and set the CENTER FREQ to measure the bias voltage.

(3) The bias voltage varies depending on the RF I/O board DC data.
The bias can be changed for each band in the maintenance mode.

Press [SHIFT] [5], [9] [4] [2] [8] [4], and [MIX TUNE] on the R3271 and select the band by inputting numerals corresponding to the CENTER FREQ.

For 3.5 to 7.5 GHz, press [BAND SELECT] [2] [Hz]

For 7.5 to 15.4 GHz, press [BAND SELECT] [3] [Hz]

For 15.4 to 23.3 GHz, press [BAND SELECT] [4] [Hz]

For 23.3 to 20.5 GHz, press [BAND SELECT] [5] [Hz]

When band selection is made, the span is set to the full span of the selected band. Therefore, press the [START] and [STOP] keys to set the zero span.
For example, if you want to set the CENTER FREQ to 5 GHz and the SPAN to zero, press [START] [5] [GHz], [STOP] [5] [GHz].
The bias voltage is changed by pressing [BIAS ADJ FIX/NAR] and turning the data knob.

CAUTION

- If SHIFT ON are pressed, the EEPROM data is rewritten and the existing data is cleared. Do not press the keys.
- When you do not know the existing data, turn off and on the R3271 power switch, and the data returns to EEPROM values. The maintenance mode is canceled at that time.

Remove the J13 connector and turn the data knob while observing the voltage of pin 1 of J13 on the DVM. If the data displayed on the screen is changed from 00 to FF, the bias voltage is changed in every band.
If the variation in voltage is within the range of −1 to +6 V, up to the RF I/O is judged normal.

[Dual Mixer Conversion Loss]

(1) Table 6-6 shows the signal loss at the IF when a signal is input to the RF IN. It is assumed that the reference level is input at the local.

Table 6-6 Dual Mixer Conversion Loss

Band	Conversion Loss
R3265 ONLY (THD294)	
0 to 3.6 GHz	13 dB
3.5 to 8 GHz	12 dB
R3271 ONLY (THD293)	
0 to 3.6 GHz	13 dB
3.5 to 7.5 GHz	18 dB
7.5 to 15.4 GHz	24 dB
15.4 to 23.3 GHz	30 dB
23.3 to 26.5 GHz	36 dB

(2) Set the span of the R3265/3271 to zero and set the CENTER FREQ to the frequency to be measured. Input to the mixer base band RF IN connector from the SG for less than 3.6 GHz less, or input to the mixer high band RF IN connector from the SG for the more than 3.6 GHz. Measure the 4231.42 MHz IF frequency for the base band, or the 421.42 MHz IF frequency for the high band with another spectrum analyzer for calculating the loss.
Input the signal level less than −20 dBm to the mixer RF IN.

6.3.3 Input Attenuator

(1) Conduct the input attenuator accuracy test in the performance test.
If the switching error seems to exceed 10 dB, it is considered that the attenuator has not been switched.

(2) Press [CPL] [ATT] on the R3265/3271. Use the [↑] and [↓] keys to switch the attenuator from 0 to 70 dB to check that a click is heard.
If no click is heard, the attenuator drive circuitry may be in failure.

(3) The voltage of each U57 and U66 on the RF I/O board is observed on the DVM oscilloscope as shown in Table 6-7.
If the voltage is as shown in Table 6-7 and the attenuator has not been switched, the attenuator may be in failure.

Table 6-7 RF I/O Board U57, J4 Status (R3265 only)

ATT setting (dB)	10 dB THRU	10 dB ATT	40 dB THRU	40 dB ATT	20 dB THRU	20 dB ATT
	U57 16 pin	U57 15 pin	U57 12 pin	U57 11 pin	U57 14 pin	U57 13 pin
	J4 1 pin	J4 2 pin	J4 3 pin	J4 4 pin	J4 5 pin	J4 6 pin
0	L	H	L	H	L	H
10	H	L	L	H	L	H
20	L	H	L	H	H	L
30	H	L	L	H	H	L
40	L	H	H	L	L	H
50	H	L	H	L	L	H
60	L	H	H	L	H	L
70	H	L	H	L	H	L

Pins 9 and 10 of J4: +24 V
Pins 7 and 8 of J4 : Not used

Table 6-7 RF I/O Board U57, U66, J3 Status (R3271 only)

ATT setting (dB)	Section 1 10 dB ATT	Section 3 THRU	Section 4 THRU	Section 2 20 dB ATT	Section 3 20 dB ATT	Section 4 20 dB ATT	Section 2 THRU	Section 1 THRU
	U57 15 pin	U57 12 pin	U66 5 pin	U57 13 pin	U57 11 pin	U66 3 pin	U57 14 pin	U57 16 pin
	J3 2 pin	J3 3 pin	J3 4 pin	J3 5 pin	J3 9 pin	J3 10 pin	J3 11 pin	J3 13 pin
0	H	L	L	H	H	H	L	L
10	L	L	L	H	H	H	L	H
20	H	L	H	H	H	L	L	L
30	L	L	H	H	H	L	L	H
40	H	L	H	L	H	L	H	L
50	L	L	H	L	H	L	H	H
60	H	H	H	L	L	L	H	L
70	L	H	H	L	L	L	H	H

Pin 6 of J3 : +24 V

Pins 1, 7, 8, 12 and 14 of J3 : Not used

6.3.4 YTF (YIG Tuned Filter)

[YTF]

(1) The center shift of the YTF can be observed when the same signals as the center frequency of R3265/3271 are entered, the ZERO SPAN mode is selected, and when the YTF SWEEP function of the Maintenance Mode is turned ON.

(2) Use the synthesized signal generator (SG) as follows:
Set the CW control of the SG to the same position as the CENTER FREQ of R3265/3271. Set the SG power level to −5 dBm. Also, set the R3265/3271 as follows:

SPAN ..... ZERO SPAN
RBW 3MHz
Sweep Time ..... 500 msec

(3) Press the [SHIFT] and [5] keys simultaneously, enter value "94284" by pressing keys [9], [4], [2], [8] and [4] in this order, and press the [YTF TUNE] and [YTF SWEEP ON/OFF] keys.

If normal, the peak waveforms of BPF comes within the ±2 div range of the center frequency on the screen (see Figure 6-5).

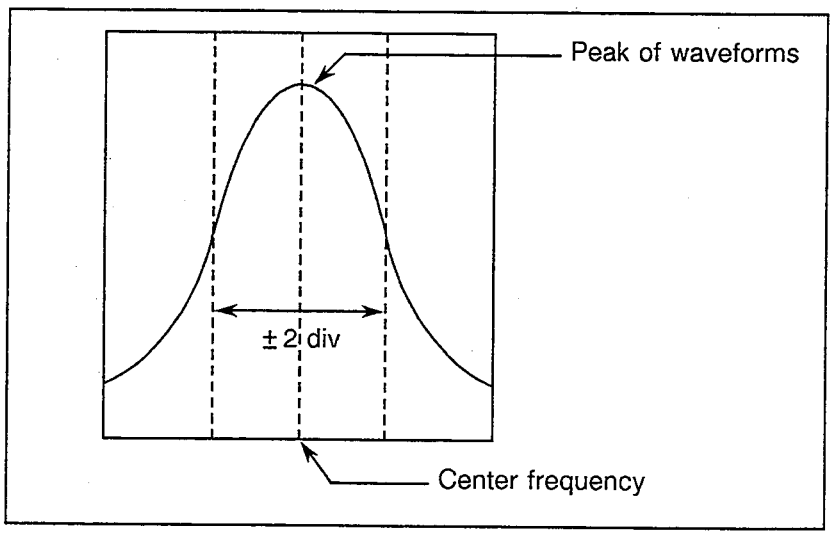


Figure 6-5 YTF Center Shift

(4) Enter the tuned frequency signals into the YTF input and make sure that the insertion loss of the output signal is within the limit defined on Table 6-8.

Table 6-8 YTF Insertion Loss

R3265 ONLY (TOP2202:DNF-002054-1)	
Band	Insertion Loss (J1→J2)
3.5 to 8.5 GHz	6 dB
R3271 ONLY (TOP2202:DNF-002055-1)	
Band	Insertion Loss (J1→J2)
3.5 to 12 GHz	6 dB
12 to 18GHz	7 dB
18 to 23.5 GHz	8 dB
23.5 to 26.5 GHz	9 dB
R3265/3271	
Band	Insertion Loss (J1→J3)
0 to 3.6 GHz	1 dB

(5) Flow the current to X in Tuning Coil of the YTF and make sure that the frequency change is within the limit defined on Table 6-9.

Table 6-9 YTF Tuning Sensitivity

	Tuning Sensitivity
R3265	21 ± 2 MHz/mA
R3271	75 ± 7 MHz/mA

[Pin Switches]

(1) The YTF has the built-in pin switch control (SW terminal) that is associated with the BAND mode setup.
Connect a digital voltmeter (DVM) to the SW terminal of the YTF and measure the voltages. They must be within the limit defined on Table 6-10 in each band.

Table 6-10 SW Terminal Voltages

Band	SW terminal voltage
0 to 3.6 GHz	+13 to +15V
3.6 GHz or more	−0.7 to −1.3V

6.3.5 Bias T

(1) The conversion loss changes (J1 to J2) according to the band selection. Table 6-11 provides the relationship between the conversion loss and control voltage. (Voltage of C1)

Table 6-11 Conversion Loss and Control Voltage

Band	Conversion loss	Control voltage
0 to 3.6 GHz	0.2×f (GHz) dB	−13 to −15V
3.6 GHz or more	10 dB or more (at 400 MHz)	+3 to +5V

(2) Set the R3265/3271 to the ZERO SPAN mode, set the CENTER FREQ value to 1 GHz or 4 GHz, and make sure that the control voltage is within the limit as defined on Table 6-11. If it is satisfied, the RF I/O board functions normally.
Note: If the band is set outside of YTF, no bias current flows. Select the band correctly.

6.3.6 Second Converter (BTF-017356, BTF-017504)

Set the CENTER FREQ value of the R3265/3271 to the 0 to 3.6 GHz band for the 2nd converter measurement.

[Conversion Loss]

(1) Enter the CAL signal to the R3265/3271 and set as follows using the PRESET key:

CENTER FREQ ..... 25 MHz
SPAN ..... 0 Hz

(2) Unplug the connector from the J11 terminal, and connect the other spectrum analyzer to the J11 terminal. Set the center frequency of this analyzer to 421.42 MHz. The signal level at this 421.52MHz frequency must be as follows:
−26 dBm for the R3265
−41 dBm for the R3271
If it is satisfied, the devices to the 2nd converter are all normal.

(3) The 2nd converter alone must have the following conversion loss.
Enter the 4231.42 MHz signals to the isolator input terminal of J12, and enter the −20 dBm or less level signals from the signal generator (SG), and make sure that the input signal level of 421.42 MHz signals at J11 is as follows:
+8 dB for the R3265
−7 dB for the R3271

(4) Make sure that the correct power voltages are supplied to the following filters:

FL15	. . . . .	−12V
FL16	. . . . .	+8V
FL17	. . . . .	−15V
FL18	. . . . .	+8V
FL19	. . . . .	−15V

If the above listed voltages are not supplied to filters FL15, FL17 and FL19, the RF I/O board or wirings have failed.
If the above listed voltages are not supplied to filters FL16 and FL18, check the regulator board (BLB-017045).

[2nd LO PLL]

(1) Connect another spectrum analyzer to J11, and set the CENTER FREQ of this analyzer to 3810.0 MHz and its SPAN to approximately 100 kHz. Now, the 2nd local leakage can be measured. Although the signal level is approximately −40 dBm and it is very small, its lock can be checked.
If signals appear at the center frequency, the 2nd PLL functions normally. If not locked, the frequency has been shifted for several megahertz.

(2) Measure the control voltage of the 2nd local VCO by using a DVM connected to the C6 terminal. The normal control voltage is 4 ±2V. If not, the lock is not set.

(3) Measure the 2nd LO OUT level of the PLL. Connect another spectrum analyzer to J10, and connect the DC power line to the C6 terminal. The voltage must be within 4 ±0.2V. Because no current flows on this terminal, it may be required to parallelly connect a resistor for small current flow.
Set the CENTER FREQ of another spectrum analyzer to 3810.0 MHz and its SPAN to 100 kHz . The 2nd local signal output level must be within the range of −5 to +4 dBm. If not, the BTF-017356 (R3265) or BTF-017504 (R3271) has failed.

(4) If the correct signals appear at J10, check the PLL board. Connect the signal cable between J10 and J7 (open the top cover of the PLB-017037).
The 200.0MHz signals are sent from the Synth block to J8. Make sure that this signal level is 0 dBm ±3 dB. If it is low, the Synth block or signal cable has failed.

(5) Make sure that the correct power voltages are supplied to the following filters:

FL9	+15V
FL10	−15V
FL11	+15V
FL12	+5V
FL13	+15V
FL14	−15V

If the above listed voltages are not supplied to the respective filters, the RF I/O board or wirings have failed.

(6) Check the 2nd sampler as follows.
Check the output of C3 capacitor at the 200 MHz level of spectrum analyzer. It must be within the range of −10 dBm ±3 dB. If not, the PLB-017027 board has failed.

(7) If the 200 MHz level signals are correct at C3 and if the 3810 MHz level signals are correct at J7, an output of approximately +12 dBm ±3 dB appear at 10 MHz level at C4.
Use a 500-ohm probe, and the signal level can be measured at C3 and C4 without disconnecting the wirings.
If the 10 MHz level signal is less than the limit, the 2nd sampler (THD296) has failed.

6.3.7 Third Converter

(1) Measure the gain of 3rd converter as follows.
Set the CENTER FREQ value of R3265/3271 to 1 GHz, and set its SPAN to 0 Hz. Enter the 421.42 MHz and −30 dBm level signals from the signal generator (SG) to the J6 terminal of the 3rd converter.

(2) Connect another spectrum analyzer to the J2 (21.42 MHz OUT) terminal of 3rd converter. Set the CENTER FREQ of this analyzer to 21.42 MHz and its SPAN to approximately 10 MHz. Measure the output level of 21.42 MHz signals of the 3rd converter.

(3) As shown on the 3rd converter signal level chart of the block diagram, the converter must have the following gain at the 421.42 MHz input signal level:
10 dB for the R3265
25 dB for the R3271

(4) If the gain is low, perform the following.
The 400.0 MHz signals are sent from the synthesizer block to the J1 terminal. Unplug the UM connector from J1, and connect another spectrum analyzer to this cable output. Set the CENTER FREQ value of this analyzer to 400 MHz and set its SPAN to approximately 200 kHz. Then, measure the signal level. If it is −5 dBm or more, the 3rd converter functions normally.

(5) Make sure that the following voltages are supplied to the corresponding filters:

FL1		−15V
FL2		0 to +6V
FL3		−1 to −13V
FL4	(0 to 3.6 GHz band)	+15V
	(Other bands)	−15V
FL5	(EXT MIXer Band)	+15V
	(Other bands)	−15V
FL6	(R3265: 3.5 to 8 GHz band)	+15V
	(R3271: 3.5 to 26.5 GHz band)	+15V
	(Other bands)	−15V
FL7	(0 to 3.6 GHz band)	+15V
	(Other bands)	−15V
FL8		−15V

If the above listed voltages are not supplied, the RF I/O board or wirings have failed.

(6) If the gain is below the limit but the voltages listed in Step (5) are supplied, the 3rd converter board (BLC-017027x01, x02) has failed.

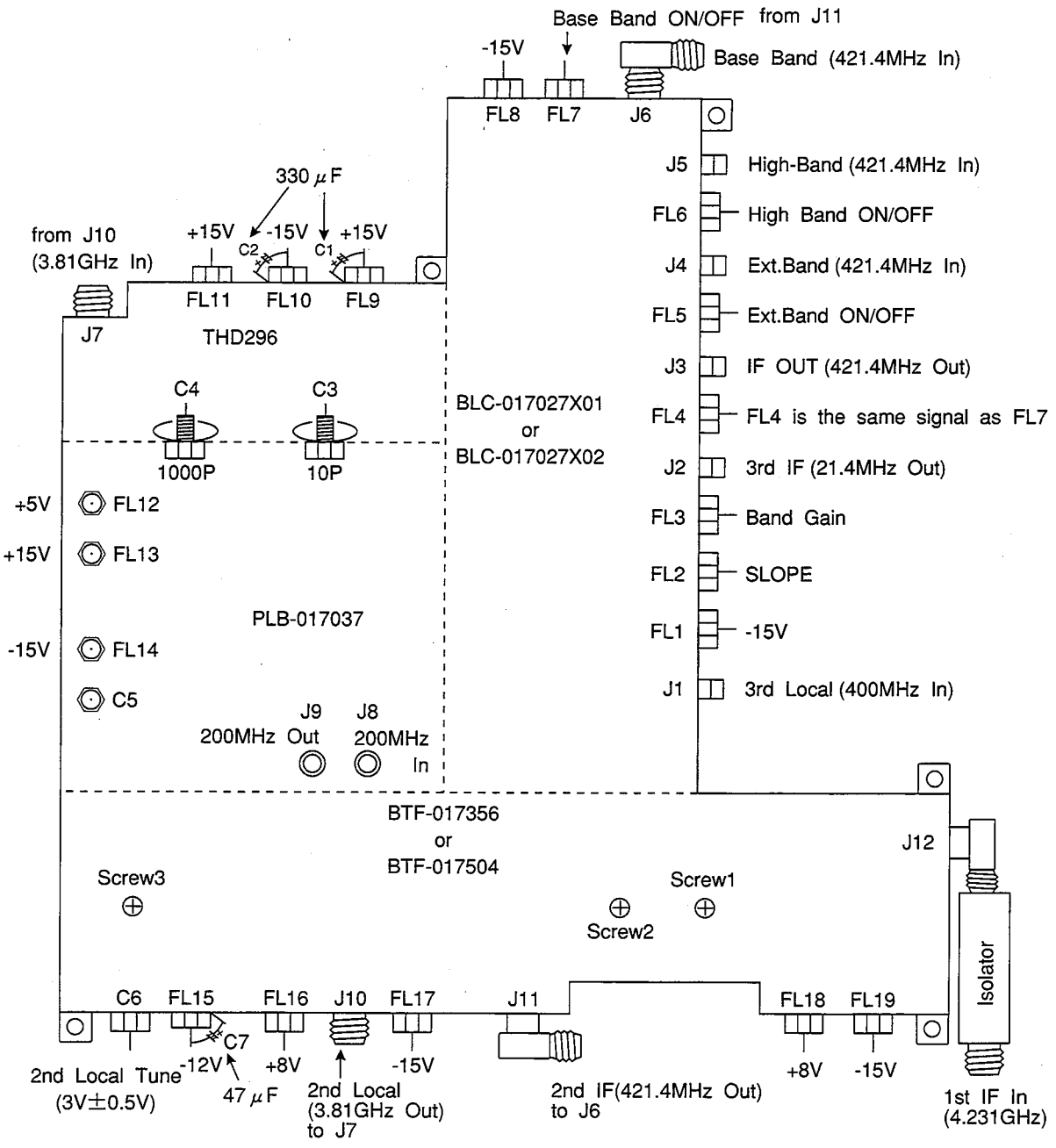
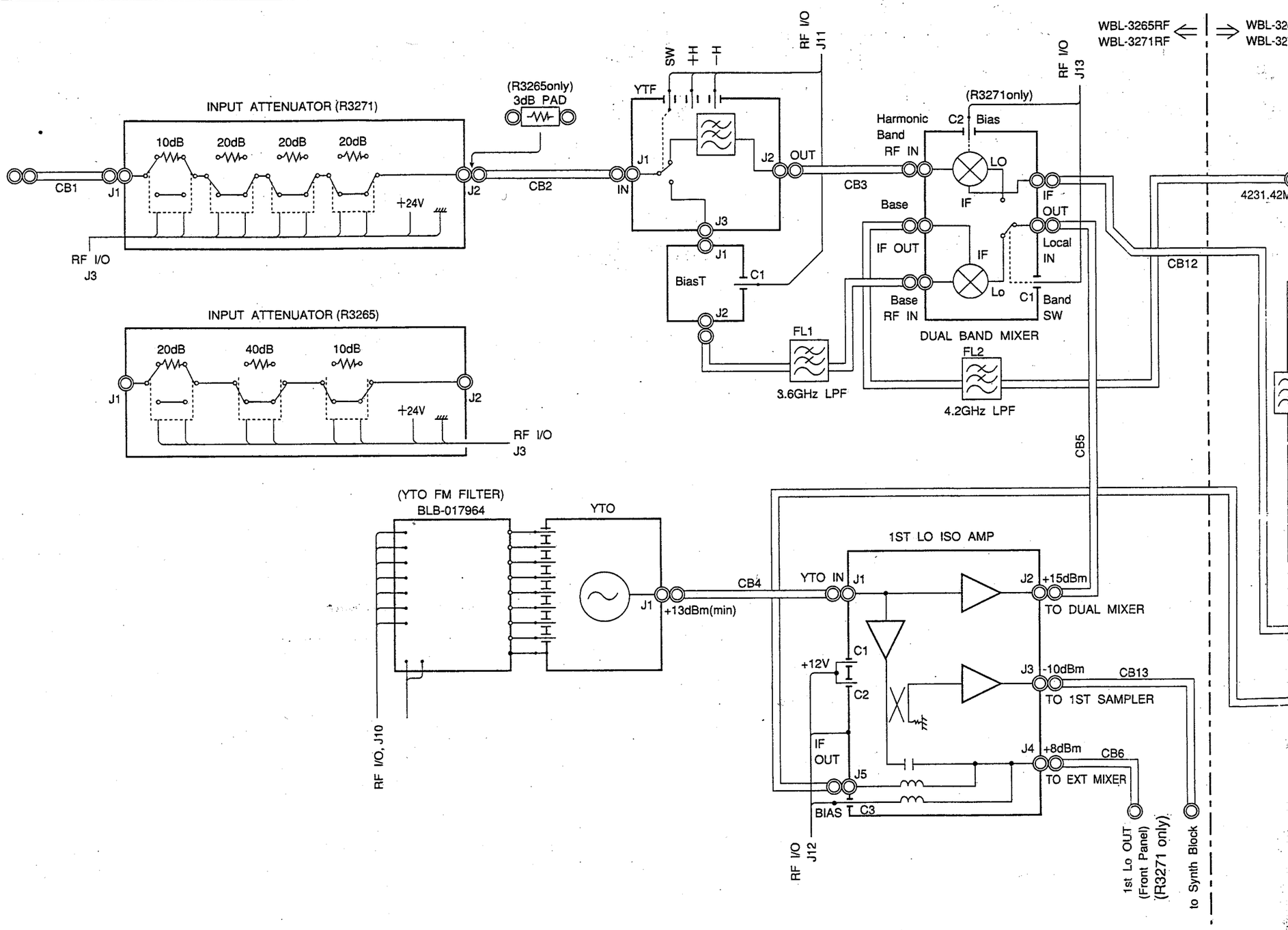
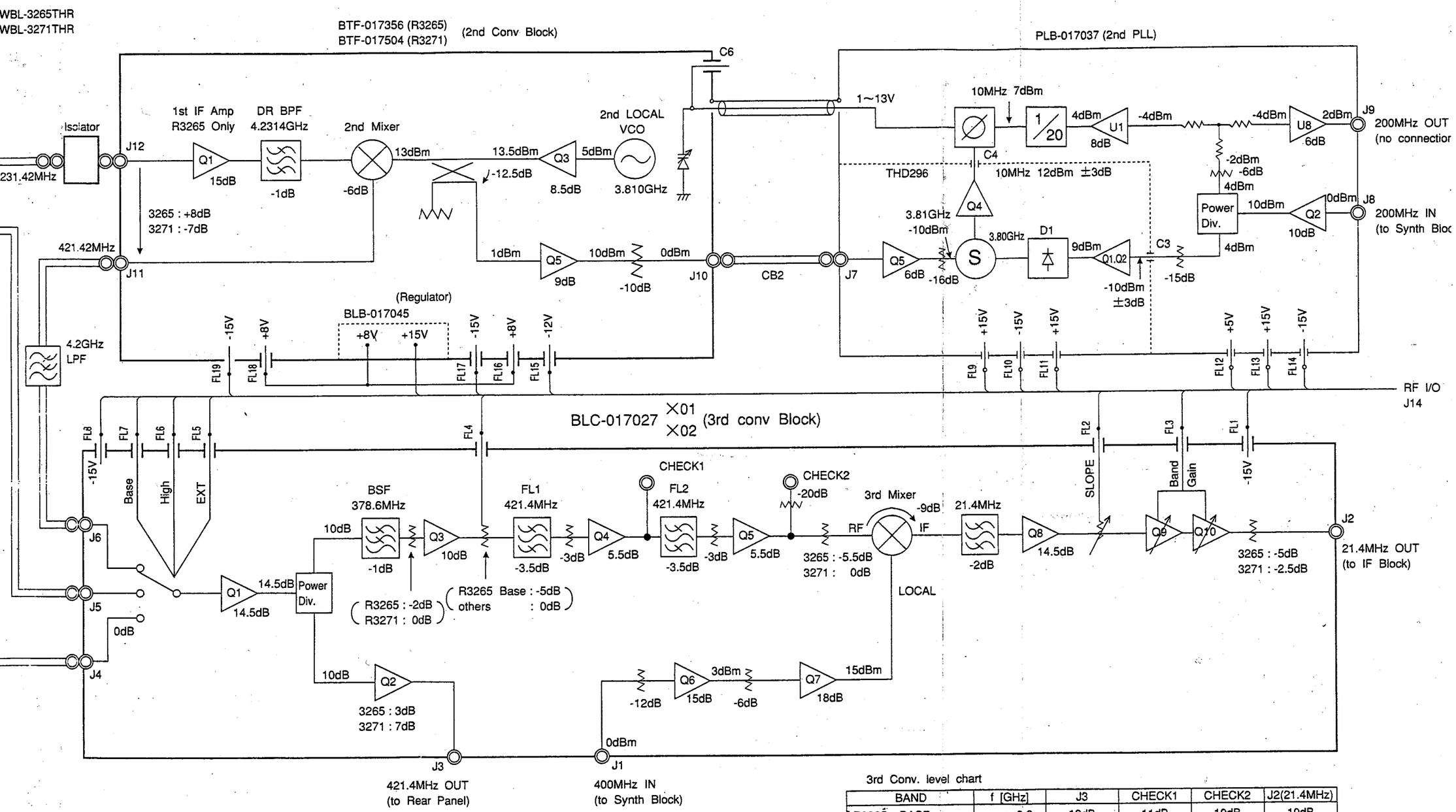


Figure 6-6 WBL-3265,3271 THR Connector


INPUT ATTENUATOR (R3271)
10dB
20dB
20dB
20dB
CB1
J1
+24V
J2
CB2
RF I/O
J3
(R3265only)
3dB PAD
IN
YTF
SW
+H
-H
J1
J2
OUT
RF I/O
J11
CB3
WBL-3265RF
WBL-3271RF
WBL-32
RF I/O
J13
(R3271only)
Harmonic
Band
RF IN
C2
Bias
LO
IF
Base
IF
OUT
J3
J1
BiasT
C1
IF OUT
IF
Local
IN
Base
RF IN
Lo
C1
Band
SW
DUAL BAND MIXER
CB12
4231.42M
J2
FL1
3.6GHz LPF
FL2
4.2GHz LPF
INPUT ATTENUATOR (R3265)
20dB
40dB
10dB
J1
+24V
J2
RF I/O
J3
CB5
(YTO FM FILTER)
BLB-017964
YTO
RF I/O, J10
J1
+13dBm(min)
CB4
1ST LO ISO AMP
YTO IN
J1
J2
+15dBm
TO DUAL MIXER
C1
+12V
C2
J3
-10dBm
CB13
TO 1ST SAMPLER
IF
OUT
J4
+8dBm
CB6
TO EXT MIXER
J5
BIAS
C3
RF I/O
J12
1st Lo OUT
(Front Panel)
(R3271 only)
to Synth Block

WBL-3265THR
WBL-3271THR



3rd Conv. level chart

BAND		f [GHz]	J3	CHECK1	CHECK2	J2(21.4MHz)
R3265	BASE	~3.6	12dB	11dB	10dB	10dB
	HIGH	3.5~8	(50Ωterm)	16dB	15dB	27dB
R3271	BASE	~3.6	16dB (50Ωterm)	19dB	18dB	25dB
	HIGH n=1	3.5~7.5				25dB
	n=2	7.4~15.4				33dB
	n=3	11.3~23				42dB
	n=4	15.2~26.5				46dB

Figure 6-7 RF Section BLCCK DIAGRAM

6.4 IF Section

6.4.1 Performance Test Failures

Failures in the IF (interface) section related performance tests can be investigated using the following information.

[IF Gain Error Performance Test]
The failure of this performance test indicates a possible problem on the R3265/3271's IF gain circuits.
For 10 Hz to 100 kHz RBW, the IF gain problems in the first 80 dB of IF gain (REF level of 0 dBm to 80 dBm with 10dB input attenuation) result from the failure of IF assembly. For 10 Hz to 100 kHz RBW, the IF gain problems in the next 60 dB of IF gain (REF level of −90 dBm to −140 dBm with 10dB input attenuation) result from the failure of LOG Assembly.
For 300 kHz to 3 MHz RBW, the IF gain problems in the first 10 dB of IF gain (REF level of 0 dBm to −10 dBm with 10dB input attenuation) result from the failure of IF assembly. For 300 kHz to 3 MHz RBW, the IF gain problems in the next 130 dB of IF gain (REF level of −20 to −140 dBm with 10dB input attenuation) result from the failure of LOG Assembly.

[Resolution Bandwidth Performance Test]
Most of the resolution bandwidth problems are the result of IF assembly failure. However, if the frequency span accuracy is outside the specifications, the resolution bandwidth are affected. Make sure that the frequency span accuracy matches the specifications.
If the R3265/3271 has the poor scale indication accuracy, its resolution bandwidth is affected. Make sure that the scale indication accuracy matches the specifications.

6.4.2 IF Assembly

The LC filter is a variable-bandwidth filter and it is used for 300 kHz to 3 MHz RBW generation. The bandwidth of the LC filter is controlled by the current generated by the DAC.
The FAR filter is a variable-bandwidth filter using the FAR resonator, and it is used for 3 kHz to 100 kHz RBW and 120 kHz and 9 kHz signal generation having 6 dB bandwidth.
The crystal filter is a variable-bandwidth filter and it is used for 10 Hz to 1 kHz RBW (analog IF) and 200 Hz signal generation having 6 dB bandwidth.
If the RBW is 100 kHz or less, the IF signals are down converted from 21.4205 MHz to 3.5795 MHz. After the signals have passed through the FAR filter or crystal filter, they are converted to 21.4205 MHz again and output to the LOG Assembly.
The step gain amplifier generates the IF gain when the reference level changes. The 0.1 dB step attenuator operates when the reference level changes at 0.1 dB step.
When the digital IF is selected, the signals are further down converted from 3.5795 MHz to 900 Hz. The 3.5786 MHz local signals used for this conversion are generated by the crystal oscillator of the IF assembly.

CAUTION

1. The test point signals of IF assembly contain DC components. It must be considered when the signals at test points are checked using the other spectrum analyzer for troubleshooting.
2. Do not short control voltages to the ground. These voltages are not short-circuit protected. Otherwise, the control circuits may be damaged.
3. Do not short power supply voltages to the ground. If done, the IF assembly circuits may be damaged.

[Resolution Bandwidth Problems]

If the resolution bandwidth is abnormal and if it may be caused by the failure of IF assembly, check the RBW control signals. The control signal status of each RBW is listed on Table 6-12. If the control signals are abnormal, the OP amp, transistors, latch IC's or others may have failed on the control circuits. The switch setting of each RBW is listed on Table 6-13.

Table 6-12 RBW Control Signals

Control Signals / RBW	U42 pin 2	U42 pin 8	U43 pin 2	Q21 pin 3	U3 pin 2	Q26 pin 3	Q26 pin 1	Q25 pin 3	Q25 pin 1	Q24 pin 3	Q24 pin 1	Q23 pin 3	Q23 pin 1	Q22 pin 3	Q22 pin 1	U43 pin 8
Digital IF	+	+	+	+1.0 V	–	–	–	–	–	+	+	–	–	–	–	–
(6 dB) 200 Hz	+	+	+	+1.0 V	–	–	–	–	–	+	–	+	–	–	–	+
(6 dB) 9 kHz	+	–	–	+1.0 V	–	–	–	–	+	–	–	–	–	–	–	+
(6 dB) 120 kHz	+	–	–	+1.0 V	+	+	–	–	–	–	–	–	–	–	–	+
10 Hz (analog IF)	+	+	+	+1.0 V	–	–	–	–	–	+	–	–	–	–	+	+
30 Hz (analog IF)	+	+	+	+1.0 V	–	–	–	–	–	+	–	–	–	+	–	+
100 Hz (analog IF)	+	+	+	+1.0 V	–	–	–	–	–	+	–	–	+	–	–	+
300 Hz	+	+	+	+1.0 V	–	–	–	–	–	+	+	–	–	–	–	+
1 kHz	+	+	+	+1.0 V	–	–	–	–	–	+	–	–	–	–	–	+
3 kHz	+	–	–	+1.0 V	–	–	–	–	–	+	–	–	–	–	–	+
10 kHz	+	–	–	+1.0 V	+	–	–	+	–	–	–	–	–	–	–	+
30 kHz	+	–	–	+1.0 V	+	–	+	–	–	–	–	–	–	–	–	+
100 kHz	+	–	–	+1.0 V	+	–	–	–	–	–	–	–	–	–	–	+
300 kHz	–	–	–	+1.0 V	+	–	–	–	–	–	–	–	–	–	–	+
1 MHz	–	–	–	+1.2 V	+	–	–	–	–	–	–	–	–	–	–	+
3 MHz	–	–	–	+1.7 V	+	–	–	–	–	–	–	–	–	–	–	+

+: +11 to +13 V (Typical)
–: –12 to –14 V (Typical)

Table 6-13 Switch Settings

SWITCHES / RBW	U1 U55	U2 U56	U12, U13 U26, U27	U11, U14 U25, U28	D42 D44	Q28 D46	U58	U62
3 MHz to 300 kHz	ON	OFF	ON	OFF	ON	OFF	ON	OFF
100 kHz to 10 kHz	OFF	ON	ON	OFF	ON	OFF	ON	OFF
3 kHz	OFF	ON	ON	OFF	OFF	ON	ON	OFF
1 kHz to 10 Hz	OFF	ON	OFF	ON	OFF	ON	ON	OFF
Digital IF	OFF	ON	OFF	ON	OFF	ON	OFF	ON

(Analog IF)

[Step Gain Problems]

Check the IF gain of the IF assembly in the following procedure.

(1) Unplug the signal cable from J1.

(2) Enter the −10 dBm, 21.42 MHz signals to J1.

(3) Press keys [PRESET], [CENTER FREQ], [2], [5], [MHz], [FREQ SPAN], [1], [0] and [MHz] in this order on the R3265/3271.

(4) Unplug the signal cable from J5.

(5) Monitor an output at J5 using another spectrum analyzer.

(6) Simultaneously decrease the output of signal generator and R3265/3271 REF LEVEL at every 10dB step.

(7) At each step, the signal displayed on the spectrum analyzer should be close to −5 dBm. (More subtle IF gain problems might require smaller signal generator and REF LEVEL setup.)

(8) If the step gain of IF assembly is abnormal, check the step gain amplifier operation. Table 6-14 provides the REF LEVEL if the input ATT is 10 dB and the operation of each step gain amp. If the step gain amp operation is abnormal, check the control signal of step gain amp. Table 6-15 lists the control signal status.

Table 6-14 Step Gain Amplifier Settings

(RBW 10 Hz to 100 kHz)

Step Gain Amp / REF LEVEL	U15 (20 dB-1)	U16 (10 dB-2/20 dB-2)	U17 (20 dB-3)	U18 (20 dB-4)	U34 (21 MHz 10 dB)
0 dBm	0 dB	0 dB	0 dB	0 dB	+11 dB
−10 dBm	0 dB	10 dB	0 dB	0 dB	+11 dB
−20 dBm	20 dB	0 dB	0 dB	0 dB	+11 dB
−30 dBm	20 dB	10 dB	0 dB	0 dB	+11 dB
−40 dBm	20 dB	20 dB	0 dB	0 dB	+11 dB
−50 dBm	20 dB	10 dB	20 dB	0 dB	+11 dB
−60 dBm	20 dB	20 dB	20 dB	0 dB	+11 dB
−70 dBm	20 dB	10 dB	20 dB	20 dB	+11 dB
−80 dBm	20 dB	10 dB	20 dB	20 dB	+21 dB

(RBW 300 kHz to 3 MHz)

Step Gain Amp / REF LEVEL	U15 (20 dB-1)	U16 (10 dB-2/20 dB-2)	U17 (20 dB-3)	U18 (20 dB-4)	U34 (21 MHz 10 dB)
0 dBm	0 dB	0 dB	0 dB	0 dB	+11 dB
−10 dBm	0 dB	0 dB	0 dB	0 dB	+21 dB

Note: The input ATT is 10 dB.

Table 6-15 Step Gain Control Signals

(RBW 10 Hz to 100 kHz)

Control signal / REF LEVEL	U49 pin2 (20 dB-1)	U48 pin8 (10 dB-2)	U49 pin8 (20 dB-2)	U50 pin2 (20 dB-3)	U50 pin8 (20 dB-4)	U51 pin16 (21 MHz 0 dB)	U51 pin15 (21 MHz 10 dB)
0 dBm	–	–	–	–	–	−14 V	−2.8 V
−10 dBm	–	+	–	–	–	−14 V	−2.8 V
−20 dBm	+	–	–	–	–	−14 V	−2.8 V
−30 dBm	+	+	–	–	–	−14 V	−2.8 V
−40 dBm	+	–	+	–	–	−14 V	−2.8 V
−50 dBm	+	+	–	+	–	−14 V	−2.8 V
−60 dBm	+	–	+	+	–	−14 V	−2.8 V
−70 dBm	+	+	–	+	+	−14 V	−2.8 V
−80 dBm	+	+	–	+	+	−7 V	−14 V

(Typical)

(RBW 300 kHz to 3 MHz)

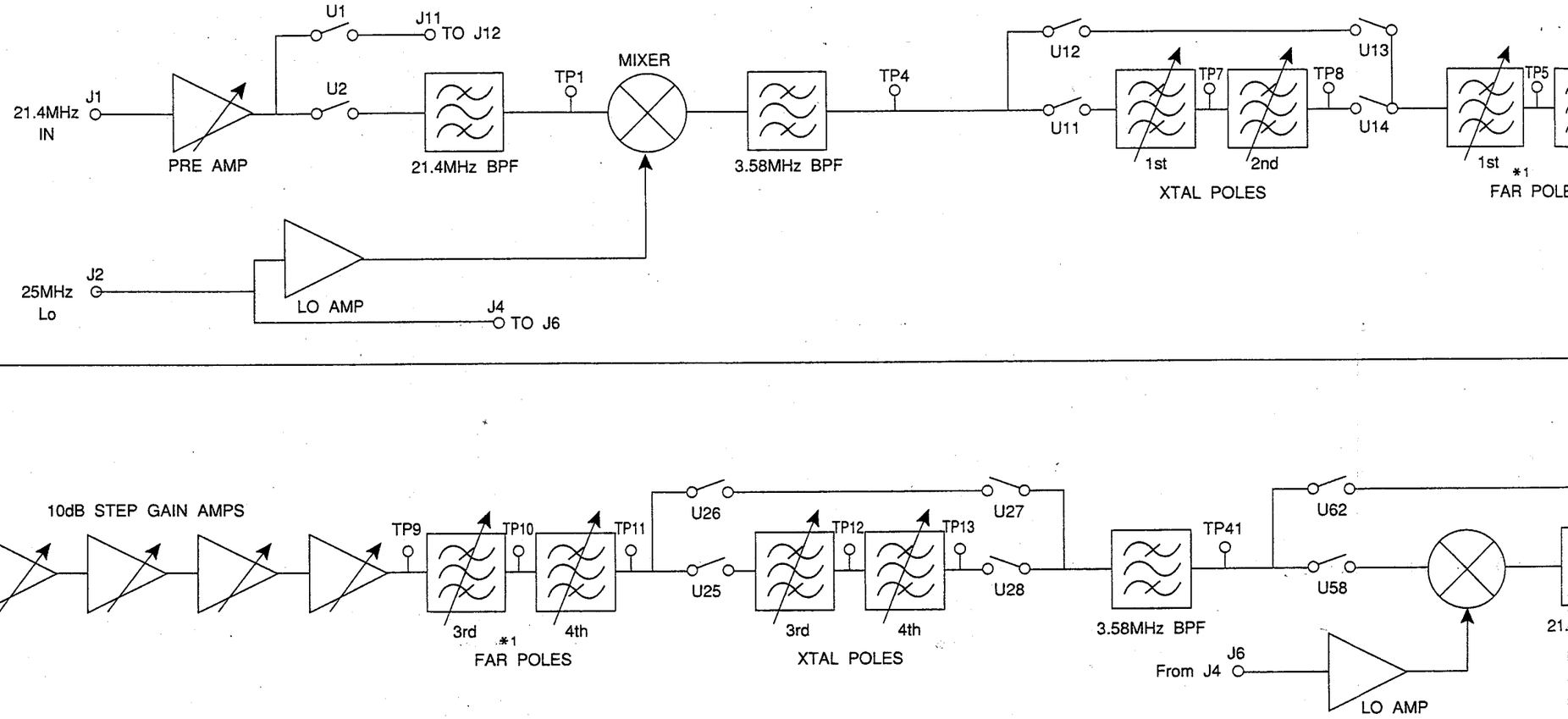
Control signal / REF LEVEL	U49 pin2	U48 pin8	U49 pin8	U50 pin2	U50 pin8	U51 pin16	U51 pin15
0 dBm	–	–	–	–	–	−14 V	−2.8 V
−10 dBm	–	–	–	–	–	−7 V	−14 V

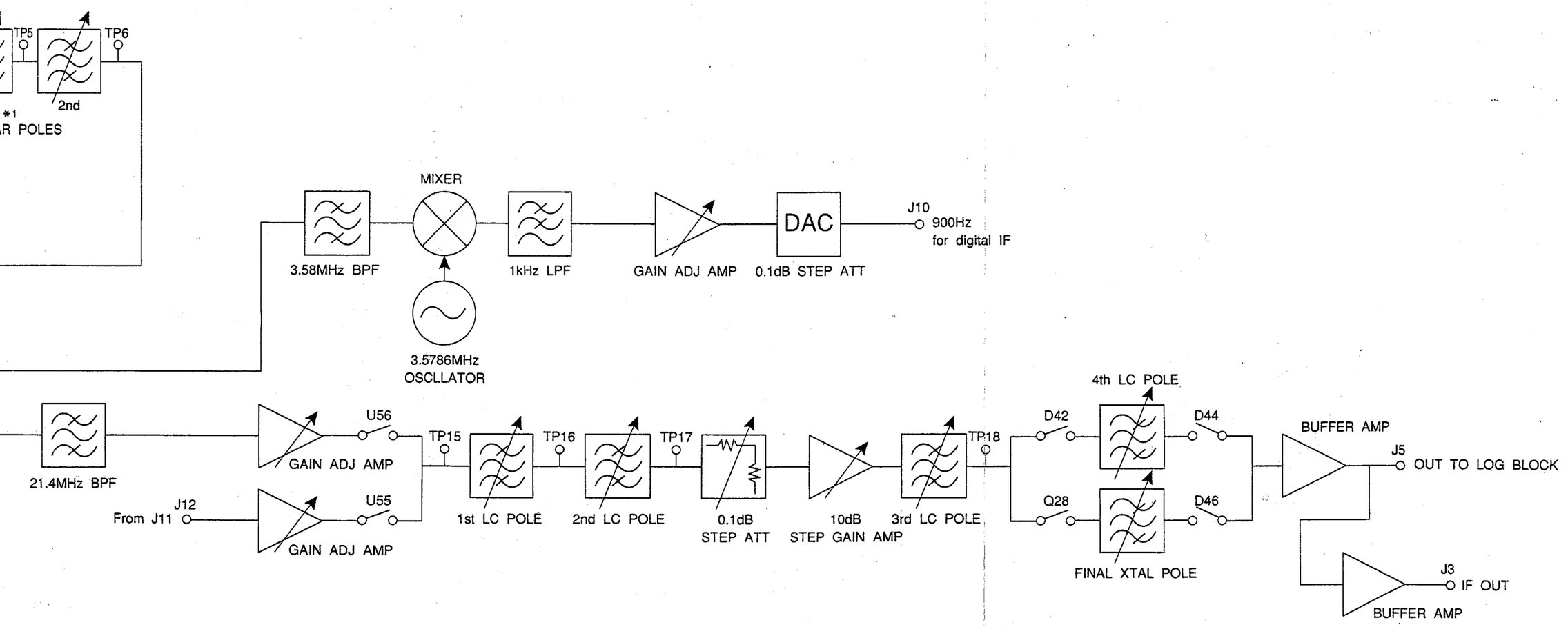
(Typical)

Note: The input ATT is 10 dB.

Symbols: –: −13.5V
+: +12.5V (Typical)

Diagram


U1
J11
TO J12
U2
21.4MHz
IN
J1
PRE AMP
21.4MHz BPF
TP1
MIXER
3.58MHz BPF
TP4
U12
U13
U11
U14
TP7
TP8
1st
2nd
XTAL POLES
TP5
1st
*1
FAR POLE
J2
25MHz
Lo
LO AMP
J4
TO J6
10dB STEP GAIN AMPS
TP9
TP10
TP11
3rd
*1
4th
FAR POLES
U26
U27
U25
U28
TP12
TP13
3rd
4th
XTAL POLES
TP41
3.58MHz BPF
U62
U58
J6
From J4
LO AMP
21.



*1 FAR : RESONATOR (CUSTOM DEVICE)

Figure 6-8 IF Section BLOCK DIAGRAM

6.5 LOG A/D Section

6.5.1 Configuration of Log Amp Block

The Log amp block consists of the Log amp having the 100 dB dynamic range, linear amp, full-wave detector, video filter, step amp, MAG amp, OP Log detector, and FM/AM demodulator. The operation of each component must be checked only after the CAL ALL test.

[Log Amp]

The LOG amp consists of 11 stages of amplifiers having the 10 dB LOG characteristics. This amp has the 100 dB dynamic range. The gain of each Log amp can be switched between 10 dB and 0 dB. All amps are set to 10 dB in the LOG mode. Make sure that the Log amp operates normally as follows.

(1) Connect the signal source cable to J8.

(2) Set the signal source as follows:

FREQUENCY 21.42MHz

(3) Set the R3265/3271 as follows:

CENTER FREQ 10MHz
SPAN 0Hz
RBW 1MHz
VBW 1kHz
REF LEVEL 0dBm (10dB/div)
MARKER ON

(4) Change the amplitude of the signal source so that the MARKER value of R3265/3271 reaches 0 dBm (reference level).

(5) Change the AMPLITUDE of the signal source at every 10 dB step from the set value to the range between −10 dB and −80 dB. Make sure that the MARKER value of R3265/3271 is within the range of −10 to −80 dBm.

(6) If the MARKER value is outside the range given in Step (5), the Log amp or detector circuit has failed.

(7) Change the RBW to 300 kHz and 100 kHz, and repeat Steps (4) and (5) for them.

(8) If the operation is incorrect for a specific RBW value, the BPF of the Log amp has failed. The BPF of the Log amp can be switched as shown on Table 6-16.

Table 6-16 Log Amp Settings

Checkpoints / RBW	U151	
	Pin 12	Pln 15
3 MHz, 1 MHz	L	H
300 kHz	H	L
100 kHz to 1 Hz	L	L

[Linear Amp]

The linear amp is used to switch the gain of 11-stage amp (Log amp) to 0 dB. The gain of linear amp itself can be changed from 0 to 80 dB at every 10 dB step according to the reference level setup. Check the correct operation of linear amp as follows.

(1) Connect the signal cable to J8.

(2) Set the signal source as follows:

FREQUENCY ..... 21.42 MHz

(3) Set the R3265/3271 as follows:

CENTER FREQ 10MHz
SPAN 0Hz
RBW 1kHz
VBW 1kHz
REF LEVEL ..... 223.6mV (Linear)
MARKER ON

(4) Change the amplitude of the signal source so that the MARKER value of R3265/3271 reaches 0 dBm (reference level).

(5) Change the amplitude of the signal source at every 10 dB step from the set value to the range between −10 dBm and −60 dBm. Also, change the REF LEVEL of the R3265/3271 in the sequence of 7.071 µV, 2.236 µV, 707.1 nV, 223.6 nV, 70.71 nV, and 22.36 nV, and make sure that the reference level is obtained.

(6) If the value is incorrect in Step (5), the linear amp or detector circuit has failed.
If the amplitude of the signal source is incorrect for a specific value, the linear amp circuit has failed.

The linear amp has been set as listed on Table 6-17 for each REF LEVEL value.

Table 6-17 Linear Amp Settings

Checkpoints / REF LEVEL	U150								U151			
	Pin 2	Pin 5	Pin 6	Pin 9	Pin 12	Pin 15	Pin 16	Pin 19	Pin 2	Pin 5	Pin 7	Pin 10
223.6 mV	L	L	L	L	L	L	L	L	L	L	L	L
7.071 μV	L	L	L	L	L	L	L	L	L	L	L	H
2.236 μV	L	H	L	L	L	L	L	L	L	L	L	H
707.1 nV	L	H	H	L	L	L	L	L	L	L	L	H
223.6 nV	L	H	H	H	L	L	L	L	L	L	L	H
70.71 nV	L	H	H	H	H	L	L	L	L	L	L	H
22.36 nV	L	H	H	H	H	H	L	L	L	L	L	H

[Full-Wave Detector]

The full-wave detector is used for full-wave rectification of 21.42MHz IF signals. The detector has approximately 40 dB of dynamic range.
Set the following to check the normal detector operations.

(1) Connect the signal source to J8.

(2) Set the signal source as follows:

FREQUENCY 21.42MHz

(3) Set the R3265/3271 as follows:

CENTER FREQ 10MHz
SPAN 0Hz
REF LEVEL . . . . . LINEAR

(4) Measure the voltage at TP15 and adjust the amplitude of signal source to have the +1V voltage.

(5) Change the amplitude of the signal source from the set value to the range between −10 dB and −40 dB at every 10 dB step. Measure the voltage at TP15 and make sure that this voltage is approximately 316 mV, 100 mV, 31.6 mV, and 10 mV.

(6) If the voltages given in Step (5) are not obtained, the linear amp or detector has failed.

[Video Filter]

The video filter locates at the stage next to the detector, and its video band can be switched within the range of 3 MHz to 1 Hz. Each video filter has been set as listed on Table 6-18.

Table 6-18 Video Filter Settings

Checkpoints / VBW	U149						
	Pin 16	Pin 15	Pin 12	Pin 9	Pin 6	Pin 5	Pin 2
3 MHz	H	L	L	L	L	H	H
1 MHz	H	L	L	L	L	H	L
300 kHz	L	H	L	L	L	H	H
100 kHz	L	H	L	L	L	H	L
30 kHz	L	L	H	L	L	H	H
10 kHz	L	L	H	L	L	H	L
3 kHz	L	L	L	H	L	H	H
1 kHz	L	L	L	H	L	H	L
300 Hz	L	H	L	L	H	L	L
100 Hz	L	H	L	L	L	L	L
30 Hz	L	L	H	L	H	L	L
10 Hz	L	L	H	L	L	L	L
3 Hz	L	L	L	H	H	L	L
1 Hz	L	L	L	H	L	L	L

Make sure that each video filter operates normally as follows.

(1) Set the R3265/3271 as follows:

CENTER FREQ 1GHz
SPAN 0Hz
RBW 3MHz
REF LEVEL 0dBm

(2) Gradually change the VBW of the R3265/3271 from 3 MHz to 1 Hz, and make sure that the noise waveforms on the screen are concentrated gradually.

(3) If the noise waveforms cannot be concentrated in Step (2), the video filter has failed.

[Step Amp]

The Step amp is used to change the gain in the LOG mode within the range of 0 to +80 dB at every 10 dB step according to the reference level. Make sure that the Step amp operates normally as follows.

(1) Connect the signal source to J8.

(2) Set the signal source as follows:

FREQUENCY 21.42MHz

(3) Set the R3265/3271 as follows:

CENTER FREQ 10MHz
SPAN 0Hz
RBW 300kHz
VBW 1kHz
REF LEVEL 0dBm
MARKER ON

(4) Change the amplitude of the signal source so that the MARKER value of R3265/3271 reaches 0 dBm (reference level).

(5) Decrease the amplitude of the signal source 10 dB from the set value, and set the REF LEVEL of the R3265/3271 to −20 dBm. Make sure that the signal is at the reference level of the screen.
Then, change the amplitude of the signal source from the set value to 80 dBm at 10dB step (that is, change it from the set value to 20 dBm, 30 dBm, 40 dBm, 50 dBm, 60 dBm, 70 dBm, and 80 dBm). Also, change the REF LEVEL of the R3265/3271 at 10 dBm step (that is, −30 dBm, −40 dBm, −50 dBm, −60 dBm, −70 dBm, −80 dBm, and −90 dBm). Make sure that the signal of each value is at the reference level of the screen.

(6) If the signal of each value is not at the reference level defined in Step (5), the Step amp has failed. The reference level has been set as shown on Table 6-19.

Table 6-19 Step Amp Settings

Checkpoints / REF LEVEL	U153			
	Pin 2	Pin 5	Pin 7	Pin 10
0 dBm	L	X	X	X
−20 dBm	H	L	L	L
−30 dBm	H	H	L	L
−40 dBm	H	L	H	L
−50 dBm	H	H	H	L
−60 dBm	H	L	L	H
−70 dBm	H	H	L	H
−80 dBm	H	L	H	H
−90 dBm	H	H	H	H

x = Don't care

[MAG Amp]

The MAG amp locates at the stage next to the video filter, and it is used for output signal level control according to the dB/div setup. The output signal level is the same during 10 dB/div and 5 dB/div setup, but they are switched to each other through software processing of data after ADC operation.
In the 2 dB/div and 1 dB/div modes, the MAG amp is used for output signal level control. While in the 0.5 dB/div, 0.2 dB/div, and 0.1 dB/div modes, the output signal level is converted logarithmically through software processing of data after ADC operation. Each MAG amp has been set as shown on Table 6-20.

Table 6-20 MAG Amp Settings

Checkpoints / dB/div	U148		
	Pin 12	Pin 15	Pin 16
10	H	L	L
5	L	H	L
2	L	L	H
1	L	L	L
0.5	H	L	L
0.2	H	L	L
0.1	H	L	L

Make sure that the MAG amp operates normally as follows.

(1) Connect the signal source to J8.

(2) Set the signal source as follows:

FREQUENCY 21.42MHz

(3) Set the R3265/3271 as follows:

CENTER FREQ 10MHz
SPAN 0Hz
RBW 1kHz
VBW 1kHz
REF LEVEL ..... 0dBm (10 dB/div)
MARKER ON

(4) Change the amplitude of the signal source so that the MARKER value of the R3265/3271 reaches 0 dBm (reference level).

(5) Change the "dB/div" value of the R3265/3271 to 5 dB/div, 2 dB/div, 1 dB/div, 0.5 dB/div, 0.2 dB/div, and 0.1 dB/div one after the other, and make sure that the waveforms indicate approximately 0 dBm at the reference level.

(6) To check the operations for each "dB/div" range of Step (5) more precisely, gradually decrease the amplitude of the signal source for 1 div of the current "dB/div" value from 0 dBm and make sure that the MARKER value decreases for 1 dB.

(7) If the values given in Steps (5) and (6) are not obtained, the MAG amp circuit has failed.

[QP Log Detector]

The QP Log detector consists of the detector, which has the charging/discharging time constant satisfying the EMC transceiver standards, and the DC log amp. It has been set as shown on Table 6-21 according to its bandwidth.

Table 6-21 QP Log Detector Settings

Checkpoints / QP RBW	U152				
	Pin 12	Pin 10	Pin 7	Pin 5	Pin 2
200 Hz	H	L	H	H	L
9 kHz	H	L	L	L	H
120 kHz	L	L	L	H	H

Make sure that the Log amp operates normally as follows.

(1) Connect the signal source to J8.

(2) Set the signal source as follows:

FREQUENCY 21.42MHz

(3) Set the R3265/3271 as follows:

CENTER FREQ 10MHz
SPAN 0Hz
MARKER ON

Press the [SHIFT] [EMC 1] , [QP] and [BW 200Hz] keys.

(4) Change the amplitude of the signal source so that the MARKER value of the R3265/3271 reaches 0 dBm (reference level).

(5) Change the amplitude of the signal source from the set value to the range between −10 dBm and −40 dBm at every 10 dB step, and make sure that the MARKER value of the R3265/3271 is within the range of approximately −10 dBm to −40 dBm.

(6) Change the QP RBW of the R3265/3271 to 9 kHz and 120 kHz, and repeat Step (5) for each of them.

(7) If the different marker values are obtained in Steps (5) and (6), the linear amp, detector, or QP Log detector has failed.

[AM/FM Demodulator]

The FM/AM demodulator circuit is used for audio signal generation. The signal output level is controlled by the DAC. The FM demodulator is used for demodulation of narrow band FM signals. The detector circuit is used for AM signal demodulation. The audio signals are output to the speaker and earphone. Check the AM/FM demodulator operations by setting as follows.

(1) Connect the signal source to J8.

(2) Set the signal source to the AM demodulation and set the R3265/3271 as follows:

CENTER FREQ	21.42MHz
AMPLITUDE	0dBm
MOD FREQ	800Hz
MOD LEVEL	80%

(3) Set the SOUND switch of R3265/3271 to AM, and set the VOLUME to #8.

(4) Make sure that the 800 Hz tone sounds on the speaker. The sound level increases when the VOLUME is increased.

(5) Set the signal source to the FM demodulation and set the R3265/3271 as follows:

CENTER FREQ	21.42MHz
AMPLITUDE	0dBm
MOD FREQ	800Hz
MOD DEVIATION	1.3kHz

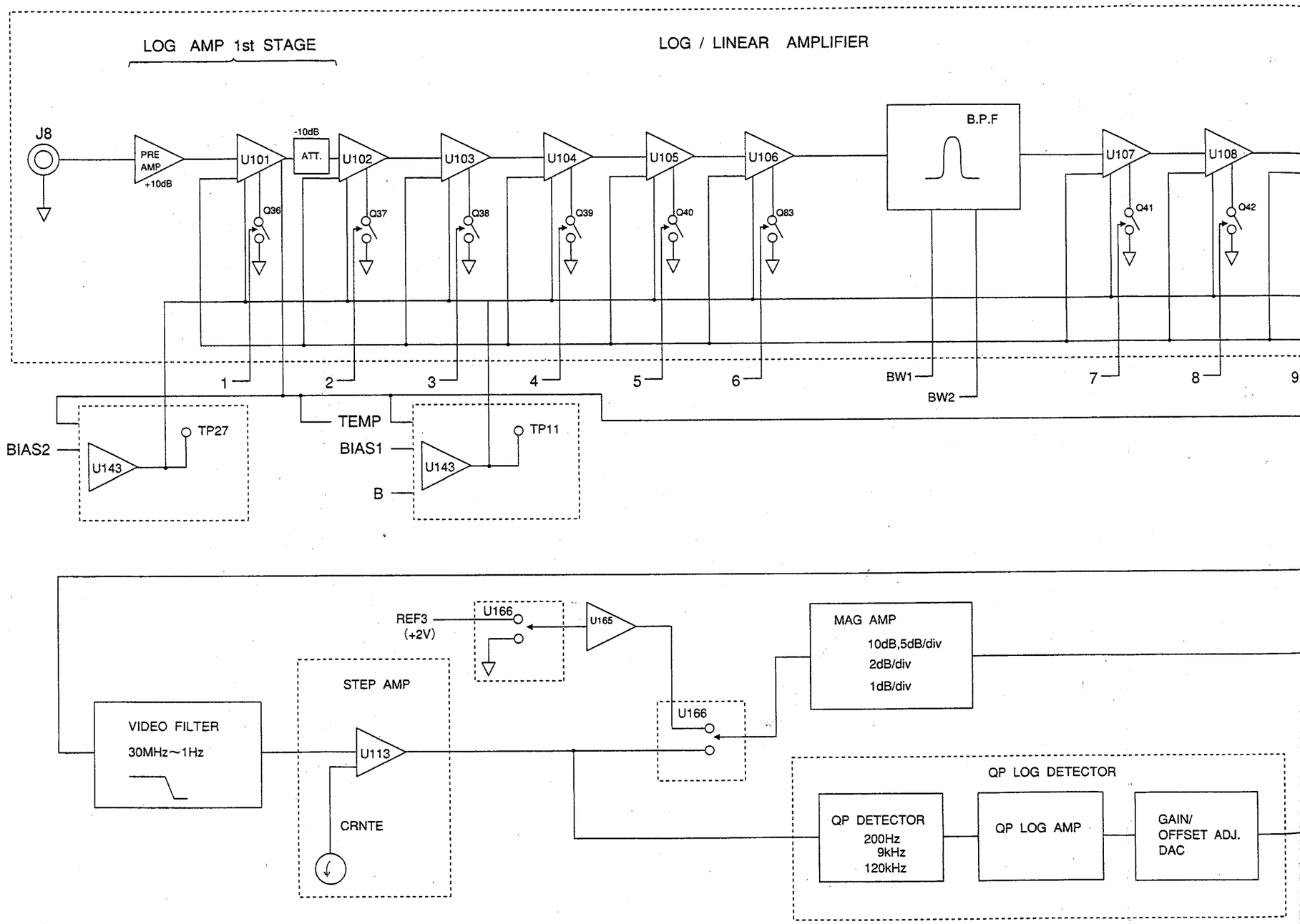
(6) Set the SOUND switch of R3265/3271 to FM, and set the VOLUME to #8.

(7) Make sure that the 800 Hz tone sounds on the speaker. The sound level increases when the VOLUME is increased.

(8) If the above operations does not occur, the FM or AM demodulator circuit has failed. The AM/FM demodulator has been set as shown on Table 6-22.

Table 6-22 AM/FM Demodulator Settings

Checkpoints / SOUND	U154		
	Pin 2	Pin 5	Pin 7
AM	L	H	H
FM	H	L	X
SOUND OFF	H	H	L


LOG AMP 1st STAGE
LOG / LINEAR AMPLIFIER
J8
PRE AMP +10dB
U101
-10dB ATT.
U102
U103
U104
U105
U106
B.P.F
U107
U108
Q36
Q37
Q38
Q39
Q40
Q83
Q41
Q42
1
2
3
4
5
6
BW1
BW2
7
8
9
TEMP
BIAS2
U143
TP27
BIAS1
U143
TP11
B
REF3 (+2V)
U166
U165
MAG AMP
10dB,5dB/div
2dB/div
1dB/div
U166
STEP AMP
VIDEO FILTER
30MHz~1Hz
U113
CRNTE
QP LOG DETECTOR
QP DETECTOR
200Hz
9kHz
120kHz
QP LOG AMP
GAIN/
OFFSET ADJ.
DAC

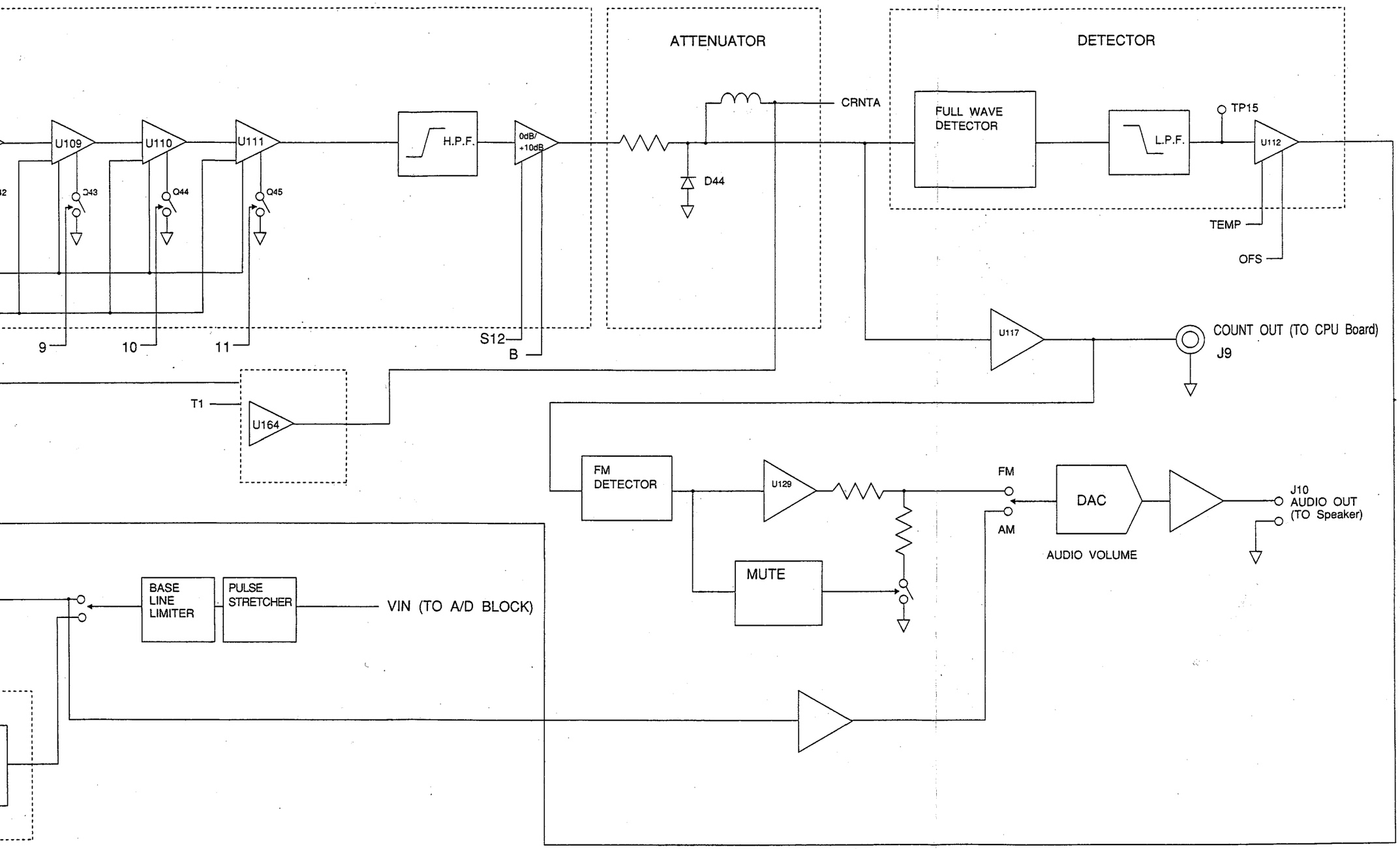


Figure 6-9 LOG AMP BLOCK DIAGRAM

6.5.2 AD Block Configuration

The AD block consists of the INPUT MUX, POSITIVE PEAK DETECTOR, NEGATIVE PEAK DETECTOR, ADC MUX, SAMPLE AND HOLD, ADC's (Low-Speed and High-Speed), VOLTAGE REFERENCE, PEAK DETECTOR RESET, ADC CONTROL, SLOPE DETECTOR, RAMP GENERATOR, and TRIGGER functional sections.
The operation of each section must be checked only after CAL ALL has been executed.

[INPUT MUX]

The INPUT MUX section switches the x1.111 AMP input of the AD block input section.

(1) Set the R3265/3271 as follows:

CENTER FREQ	1GHz
SPAN	0Hz
RBW	3MHz
VBW	3MHz

(2) Make sure that signals at pins 1, 15 and 16 of U1 are low. (VIN)

(3) Set the R3265/3271 as follows:

CENTER FREQ	1GHz
SPAN	1Hz
RBW	30Hz

(4) Make sure that signals are low at pins 1 and 15 of U1 but high at pin 16 of U1. (IF)

(5) Otherwise, the ADC CONTROL has failed.

[POSITIVE/NEGATIVE PEAK DETECTOR]

The following describes HIGH-SPEED POSITIVE PEAK DETECTOR 1. However, this description can also apply to HIGH-SPEED POSITIVE PEAK DETECTOR 2, LOW-SPEED POSITIVE PEAK DETECTOR, and HIGH/LOW-SPEED NEGATIVE PEAK DETECTOR.
HIGH-SPEED POSITIVE PEAK DETECTOR 1 consists of the input amp, output buffer (U3), detector diodes (D101, D2), hold capacitor (C20), and buffer FET (Q2) of the hold capacitor, The total gain is equal to 1, and the output (appearing at pin 9 of U3) is fed back to pin 4 of U3. The peak detector is reset by Q1.

(1) Set the R3265/3271 as follows:

CENTER FREQ	1GHz
SPAN	0Hz
RBW	3MHz
VBW	3MHz
dB/div	10dB/div

(2) Perform Steps ① to ⑤ and check the results. If these requirements are not satisfied, the positive/negative peak detector may have failed. Check the detector in the sequence after Step (3).

① The peak-to-peak noise width is approximately 2 Div in the Positive-Negative Detector mode. Record the top and bottom signal level of the displayed noise waveforms.

② Select the Positive Peak Detector mode.

③ Make sure that the noise width is approximately 1/3 Div p-p. Also, make sure that the noise level is NOT GREATER than the top level of signal in the Positive-Negative Detector mode.

④ Select the Negative Peak Detector mode. Make sure that the noise width is approximately 1/3 Div p-p. Also, make sure that the noise level is NOT SMALLER than the bottom level of signal in the Positive-Negative Detector mode.

⑤ Select the Sample Detector mode. Make sure that the noise level is between the top and bottom signal levels in the Positive-Negative Detector mode.

(3) Connect cables to the CAL OUT and INPUT terminals at the front panel of R3265/3271. Set the system as follows:

CENTER FREQ	25 MHz
SPAN	0 Hz
Sweep time	50 msec
DETECTOR MODE	Posi-Nega

(4) Simultaneously monitor waveforms of signals appearing at pins 3 and 9 of U3 on the oscilloscope.

(5) Gradually change the signal reference level from −10 dBm to +30 dBm at every 10 dBm, and make sure that the voltage of signals at pins 3 and 9 of U3 changes to 2 volts to 1.2 volts at every 200 mV.

(6) If the output voltages (at pins 3 and 9 of U3) of the peak detector do not change, check the reset pulse at pin 8 of U41. The reset pulse must be TTL negative and its width must be approximately 500 nsec for every 71 µs.

(7) If the reset pulse is not output, the PEAK DETECTOR RESET or ADC CONTROL has failed. If the reset pulse is output, check the gate of Q1. Its pulse must be positive and change from −10 volts to +15 volts.

(8) If the anode of D101 and cathode of D2 of the peak detector are short-circuited to each other, the detector operates as the unity gain amp. This amp has the flat waveforms of signals of pins 3 and 9 of U3. If the peak detector continues to operate as the unity gain amp, the D101, D2 and/or Q1 have failed.

[ADC MUX]

The ADC MUX switches the signal input to the ADC.

(1) Set the R3265/3271 as follows:

CENTER FREQ 1GHz
SPAN 0Hz
RBW 3MHz
VBW 3MHz

(2) Make sure that the signals appearing at pins 1, 8, 9 and 16 of U12 have the logic level as defined on Table 6-23.

Table 6-23 ADC MUX Setup

Checkpoint / Detector Mode	Pin 1 of U12	Pin 8 of U12	Pin 9 of U12	Pin 16 of U12
SAMPLE	H	H	L	H
POSI	L	H	H	H
NEGA	H	H	H	L

(3) Set the R3265/3271 as follows:

CENTER FREQ 1GHz
SPAN 1kHz
RBW 30Hz

(4) Make sure that the signals at pins 1, 9 and 12 of U12 are high but the signal at pin 8 is low. (FFT)

(5) Otherwise, the ADC CONTROL has failed.

[SAMPLE AND HOLD]

The SAMPLE AND HOLD holds the input signal of LOW-SPEED ADC before the ADC starts, and it samples the signal after AD conversion. Check the normal operation in the following steps.

(1) Set the R3265/3271 as follows:

CENTER FREQ	1GHz
SPAN	0Hz
DETECTOR MODE	SAMPLE
REF LEVEL	−70dBm
SWEEP TIME	50msec
dB/div	2dB/div

(2) Do not enter any signal in the input terminals of R3265/3271. The noise will appear on the entire screen of R3265/3271.

(3) Trigger the rise edge of signal appearing at pin 14 of U13 on the oscilloscope.

(4) Observe the waveforms of signal appearing at pin 7 of U13 on the oscilloscope. The waveforms must be random noise, and its average level must be approximately +1.7V. Make sure that the noise waveforms are flat on the oscilloscope when the HLD signal is high.

(5) If the requirements of Steps (2) to (4) are not satisfied, the SAMPLE AND HOLD (U13) and/or ADC CONTROL have failed.

[ADC Configuration]

The ADC section switches the ADC and CONTROL circuits to each other according to the SWEEP TIME and SPAN setup.

Table 6-24 SWEEP TIME and SPAN Setup Conditions

SWEEP TIME	1000 sec to 20 msec	19 msec to50 µs
SPAN	FULL SPAN~ZERO SPAN	ZERO SPAN
ADC RESOLUTION	16 BIT (U15)	8 BIT (U23)
DETECTOR MODE	POSI-NEGA POSI NEGA SAMPLE	SAMPLE
S/H	Yes (U13)	No
TRIGGER MODE	FREE RUN LINE VIDEO TV-V EXT	FREE RUN LINE VIDEO TV-V TV-H EXT

When the SWEEP TIME mode of 1000 sec to 20 msec (LOW-SPEED ADC) is selected, the system consists of the S/H, 16-bit ADC, and DATA LATCH circuits. It is controlled by the AD CONTROL circuit.

Four inputs are controlled by the ADC MUX. They are POSITIVE PEAK DETECTOR, NEGATIVE PEAK DETECTOR, SAMPLE DETECTOR, and FFT.

When the SWEEP TIME mode of 19 msec to 50 µs (HIGH-SPEED ADC) is selected, the system consists of the 8-bit ADC, DATA LATCH, SRAM, 3-STATE BUS TRANSCEIVER, COUNTER, and DATA SELECTOR. It is controlled by the AD CONTROL circuit.

[ADC (LOW-SPEED, HIGH-SPEED)]

The 16-bit ADC (LOW-SPEED ADC) and 8-bit ADC (HIGH-SPEED ADC) are switched to each other according to the specified sweep time. The following checks whether the ADC operates normally or not.

(1) Set the R3265/3271 as follows:

CENTER FREQ	1GHz
SPAN	0Hz
SWP TIME	50msec

(2) Observe the signal of pin 20 (CLOCK) of U15 on the oscilloscope and check the 4 MHz TTL signal level on the scope.

(3) Observe the signal of pin 1 (ADSTART) of U15 and check the negative pulse having the width of approximately 500 nsec for every 71 µs.

(4) Make sure that signals at pins 21, 22, 24 and 32 of U15 are low but signals at pins 23 and 34 of U15 are high.

(5) If the requirements of Steps (2) to (4) are not satisfied, check the ADC CONTROL.

(6) Observe the signal of pin 38 (EOC) of U15 and check the negative pulse having the width of approximately 1 µs for every 71µs. If these waveforms are not observed, the U15 or ADC CONTROL has failed.

(7) Observe the signal of pin 28 (REF) of U15 and check the +4.5V constant voltage. If this voltage is not output, check the VOLTAGE REFERENCE.

(8) Set the R3265/3271 as follows and check the HIGH-SPEED ADC operation.

CENTER FREQ	1GHz
SPAN	0Hz
SWP TIME	10msec

(9) Observe the signal of pin 10 (CLK) of U23 on the oscilloscope and check the 70 kHz TTL level signal.

(10) Observe the signal of pin 1 (*ADACQ) of U24 and check the negative pulse having the width of approximately 12 ms.

(11) If the specified waveforms are not observed in Steps (9) and (10), the ADC CONTROL has failed.

(12)Observe the signal of pin 15 (VRT) of U23 and check the +5 V constant voltage.

(13)Observe the signal of pin 19 (VRB) of U23 and check the +3 V constant voltage.

(14)If the specified voltage is not output in Steps (12) and (13), the VOLTAGE REFERENCE has failed.

[VOLTAGE REFERENCE]

The VOLTAGE REFERENCE circuit generates 6 types of voltages from the +6.3V reference voltage of.U44 (DAC).

(1) Observe the signal of pin 24 of U44 and make sure that the voltage is within +6.3 ±0.3V. If not, the U44 has failed.

(2) Make sure that the voltage is +2V at pin 1 of U55, +4.5V at pin 7, −10V at pin 8, and +10V at pin 14. If not, the U55 or the peripheral circuits have failed.

(3) Make sure that the voltage is +5V at the collector of Q13 and +3V at the collector of Q14. If not, the Q13, Q14 or its peripheral circuits have failed.

[PEAK DETECTOR RESET]

(1) Press the PRESET key of the R3265/3271 and set the parameters as follows:

CENTER FREQ 25MHz
SPAN 0Hz
SWEEP TIME 50msec
DETECTOR MODE ..... POSI-NEGA

(2) Make sure that the TTL negative signal appears at SP1 (pin 9 of U60) and the 500nsec pulses are output every 71 µs.

(3) Make sure that the TTL positive signal appears at Z (pin 10 of U60) and the 50msec pulses are output.

(4) Make sure that signal at points SPL1 (pin 16 of U7) and SPL2 (pin 1 of U7) are as those defined on Table 6-25. The signal TTL level must change as follows:

Table 6-25 PEAK DETECTOR Signal Levels

Check point / Detector mode	SPL1	SPL2
POSI-NEGA	HIGH	LOW
SAMPLE	71 µs pulse for every approx. 143 µs	71 µs pulse for every approx. 143 µs
POSI PEAK	71 µs pulse for every approx. 143 µs	71 µs pulse for every approx. 143 µs
NEGA PEAK	71 µs pulse for every approx. 143 µs	71 µs pulse for every approx. 143 µs

(5) If the requirements of Steps (2) to (4) are not satisfied, the ADC CONTROL circuit has failed.

[ADC CONTROL]

The ADC CONTROL circuit controls signal timing of all logic circuits of AD blocks such as PEAK DETECTOR RESET, SAMPLE AND HOLD, and ADC. The following checks the normal operation of ADC CONTROL circuit.

(1) Set the R3265/3271 as follows:

CENTER FREQ	1GHz
SPAN	0Hz
SWEEP TIME	50msec

(2) Observe the signal of pin 20 (CLKO) of U43 on the oscilloscope and make sure that this is the 20 MHz TTL level signal.

(3) Observe the signal of pin 4 (*STPAA) of U43 on the oscilloscope and make sure that this signal is TTL high.

(4) Observe the signal of pin 19 (*RESET) of U43 on the oscilloscope and make sure that this signal is TTL high.

(5) Observe the signal of pin 5 (*ADTRIG) of U43 on the oscilloscope and make sure that this signal is the 500nsec wide negative pulses for every 71 µs. The sweep time is 700 msec.

(6) Observe the signal of pin 7 (4M) of U43 on the oscilloscope and make sure that this is the 4 MHz TTL level signal.

(7) Observe the signal of pin 63 (*BR) of U20 on the oscilloscope and make sure that this signal is the 400 to 700-nsec wide negative pulses for every 71 µs.

(8) Observe the signal of pin 8 (*BGACK) of U20 on the oscilloscope and make sure that this signal is 1 µs wide negative pulses for every 71 µs.

(9) Observe the signal of pin 19 (*ADBG) of U20 on the oscilloscope and make sure that this signal is the 500-nsec wide negative pulses for every 71 µs.

(10) Set the R3265/3271 as follows:

CENTER FREQ	1GHz
SPAN	0Hz
SWEEP TIME	10msec

(11) Observe the signal of pin 20 (CLKO) of U43 on the oscilloscope and make sure that this is the 14 MHz TTL level signal.

(12)Observe the signal of pin 6 (CLKA) of U43 on the oscilloscope and make sure that this is the 70 kHz TTL level signal.

(13)If the specified requirements are not satisfied in Steps (2) to (12), the U43, U20, or U21 has failed.

[SLOPE DETECTOR]

The SLOPE DETECTOR selects the POSI DETECTOR or NEGA DETECTOR signals to be converted from analog into digital form in the POSI-NEGA detector mode. The input signals are detected by three comparators of U35, U36 and U85, and the next display detector is selected by the U20 built-in circuit.

U36 compares the input signal with the signal after S/H stage. If the input signal is higher than the signal after S/H, the POSI DETECTOR signal is selected for ADC. If the input signal is lower than the signal after S/H, the NEGA DETECTOR signal is selected for ADC.

U35 detects the input signal in the POSI DETECTOR output mode, and U85 detects the input in the POSI DETECTOR pulse wave mode for correct pulse wave display.

[RAMP GENERATOR]

The 20 MHz reference clock is divided at the built-in counter of U43 (GATE ARRAY), the 14-bit saw-tooth wave digital patterns are generated, and they are converted into analog signals by U44 (DAC). They are RAMP signals. U43 is used for Z signal generation and ADC control.

(1) Set the R3265/3271 as follows:

CENTER FREQ 1GHz
SPAN 0Hz
SWEEP MODE 50msec

(2) Observe the signal of pin 4 (*STPAA) of U43 on the oscilloscope and make sure that this signal is TTL high.

(3) Observe the signal of pin 19 (*RESET) of U43 on the oscilloscope and make sure that this signal is TTL high.

(4) Observe the signal of pin 20 (CLKO) of U43 on the oscilloscope and make sure that this is the 20 MHz TTL signal.

(5) Observe the signal of pin 17 of U43 on the oscilloscope and make sure that this signal has the same waveforms as shown in Figure 6-10.

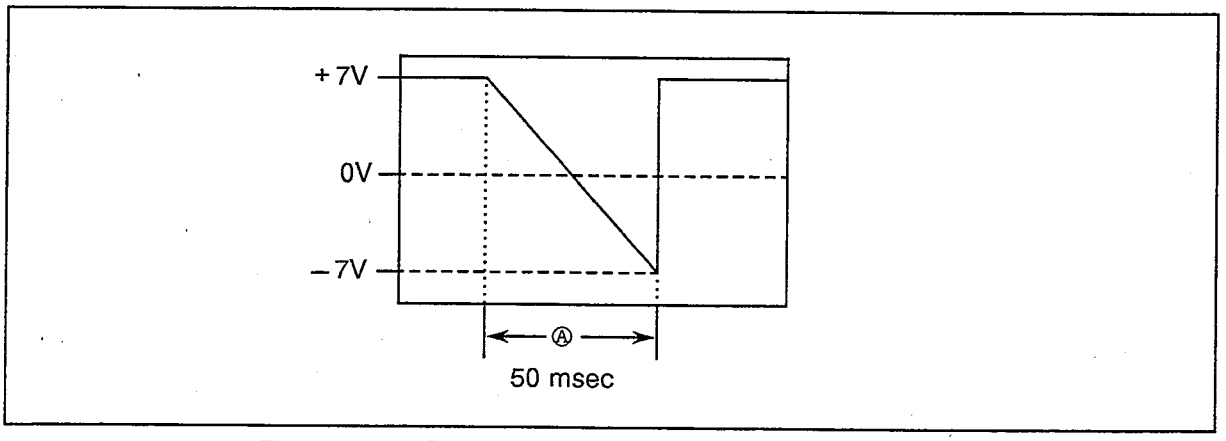


Figure 6-10 Output Waveform of Signal at Pin 17 of U43

(6) Observe the signal of pin 2 (RAMP) of J7 on the oscilloscope and make sure that this signal has the same waveforms as shown in Figure 6-11.

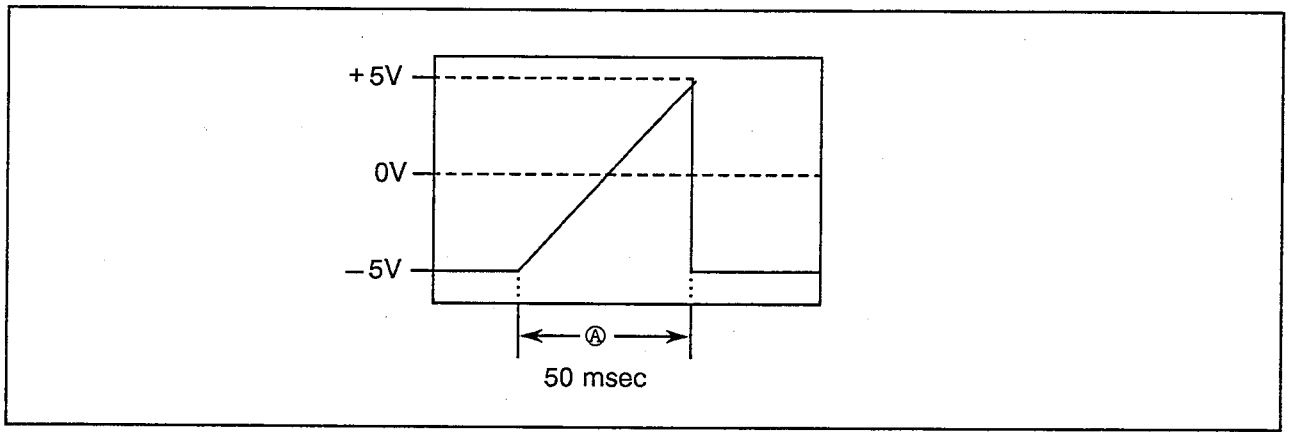


Figure 6-11 Output Waveform of Signal at Pin 2 of J7

(7) Observe the signal of pin 2 (Z) of U43 on the oscilloscope and make sure that this is the TTL level signal during period Ⓐ of Step (6). Also, make sure that this signal is low during other period.

(8) Change the SWEEP TIME to 100 msec and make sure that the sweep time is kept to 100 msec during period Ⓐ of Steps (5), (6) and (7). (The time of period Ⓐ varies in proportional to the SWEEP TIME if it is within 1000 sec to 20 msec.)

(9) If the requirements defined in Steps (2) to (8) are not satisfied, the U43, U20 or U21 has failed.

[TRIGGER]

The FREE RUN, LINE, VIDEO, or EXT trigger signal is selected by the built-in MUX of U43 and U20 which have been provided for the LOW and HIGH-SPEED ADC. The TV-V trigger signal is generated when the VIDEO signal is passed through the LPF. Also, the TV-H trigger signal is generated when the VSYNC signal of the TV SYNC SEPARATOR (U53) is counted by the built-in counter of U20, The LINE trigger signal is synchronized with the power frequency sent from the power unit. The following checks the normal operation of TRIGGER circuit.

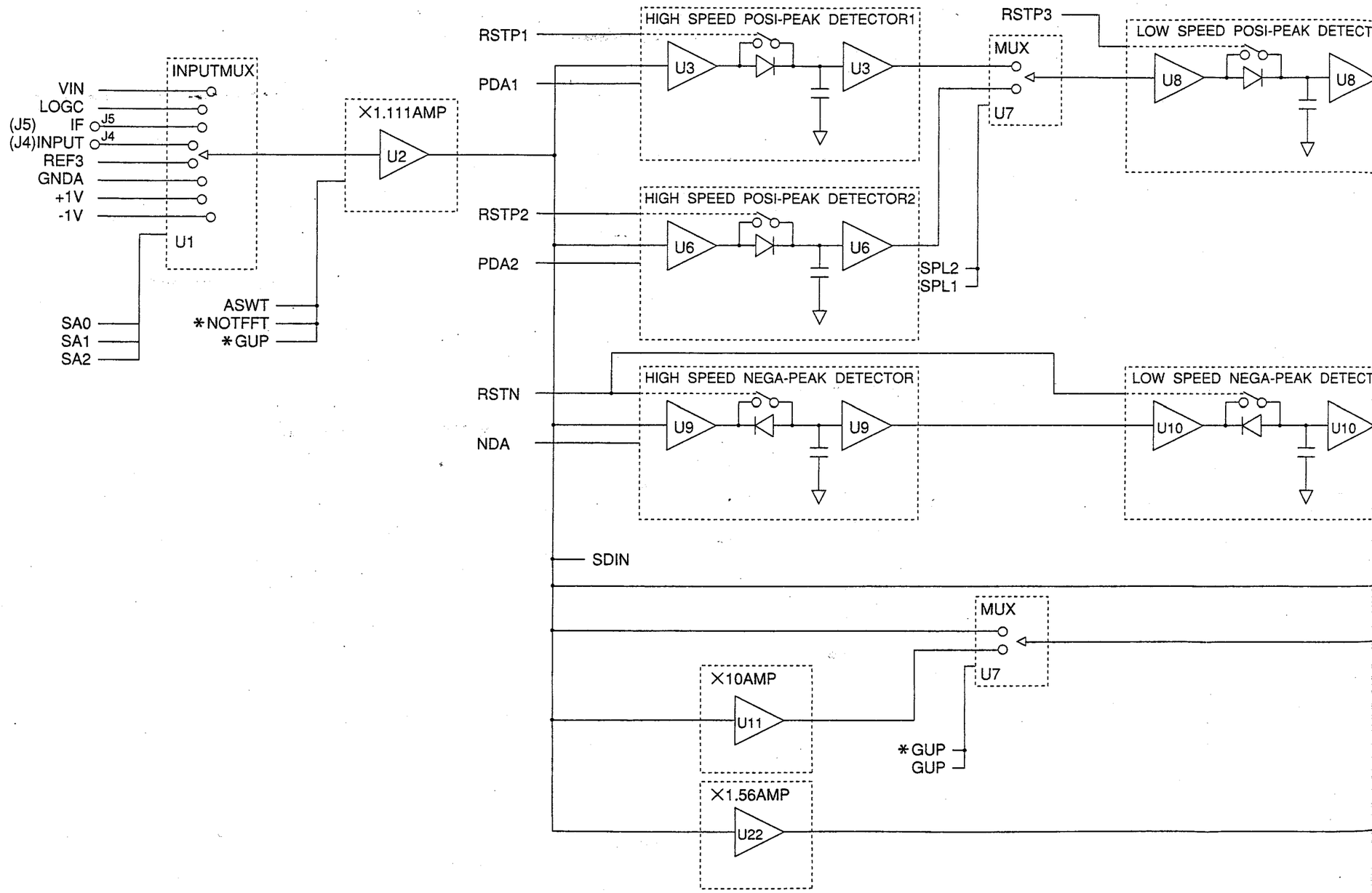
(1) Press the [MENU] key of the R3265/3271 and set as follows:

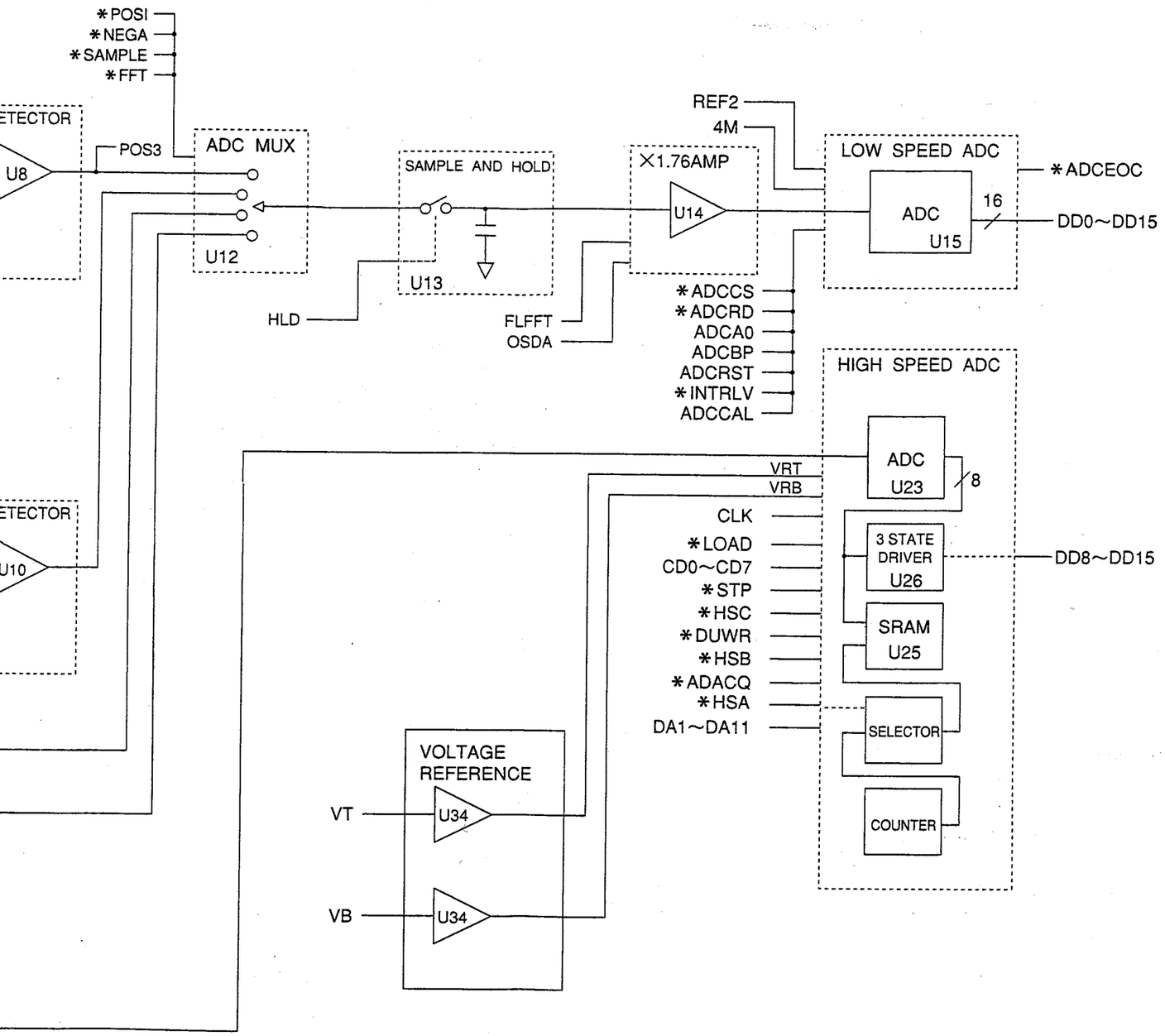
TRIG . . . . . VIDEO

(2) Change the TRIGGER level by pressing the [↓] and [↑] keys.

(3) Measure the signal voltage at pin 5 of U49 and make sure that the TRIGGER LEVEL changes at every 200mV step to +2V at the reference level on the screen or 0V at the bottom of the screen. If not, the TRIGGER circuit or ADC CONTROL has failed.

(4) Observe the signal of pin 2 of U88 on the oscilloscope and make sure that this is the TTL-level power frequency signal. If not, the TRIGGER circuit or power unit has failed.


INPUTMUX
VIN
LOGC
(J5) IF
(J4)INPUT
REF3
GNDA
+1V
-1V
U1
J5
J4
SA0
SA1
SA2
ASWT
*NOTFFT
*GUP
×1.111AMP
U2
RSTP1
PDA1
RSTP2
PDA2
RSTN
NDA
SDIN
HIGH SPEED POSI-PEAK DETECTOR1
U3
U3
HIGH SPEED POSI-PEAK DETECTOR2
U6
U6
HIGH SPEED NEGA-PEAK DETECTOR
U9
U9
MUX
U7
RSTP3
LOW SPEED POSI-PEAK DETECT
U8
U8
SPL2
SPL1
LOW SPEED NEGA-PEAK DETECT
U10
U10
MUX
U7
×10AMP
U11
*GUP
GUP
×1.56AMP
U22



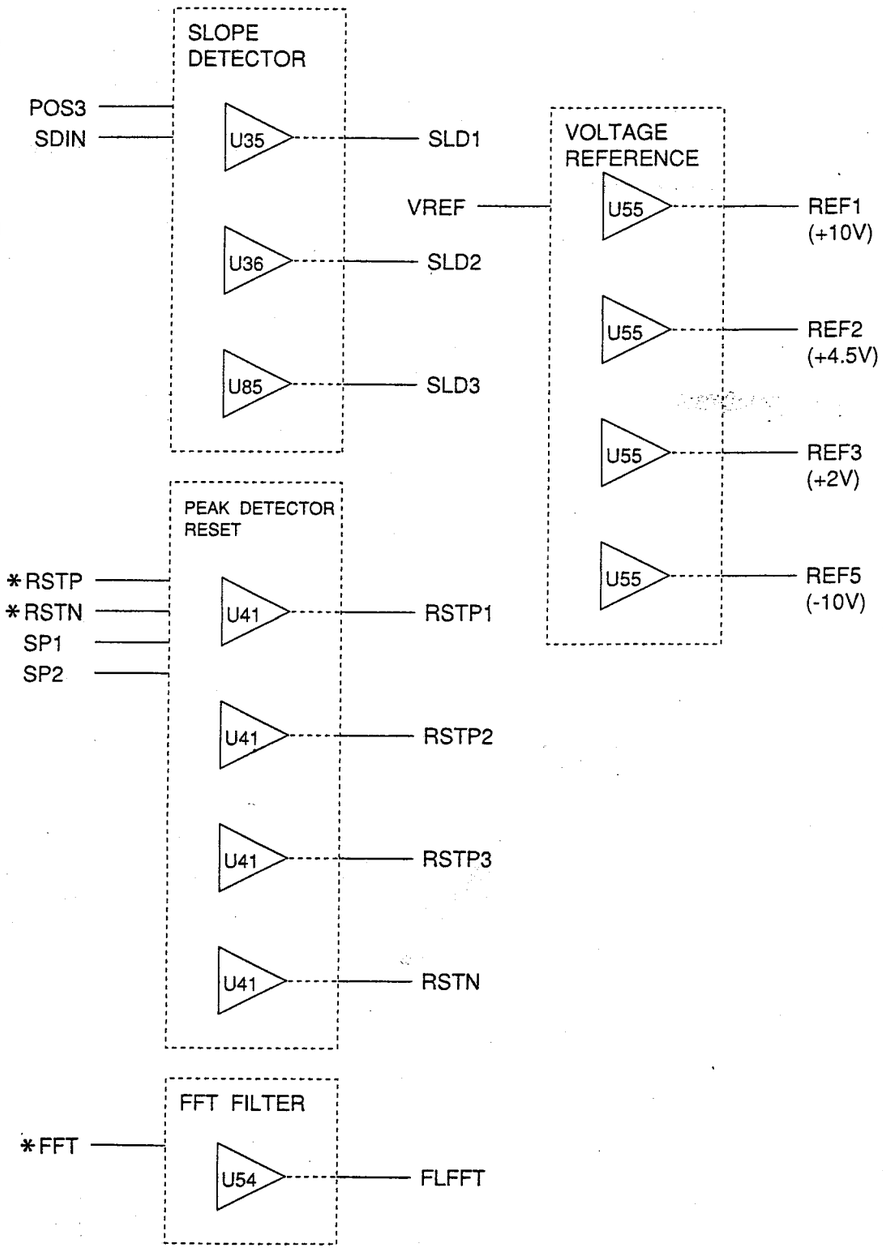
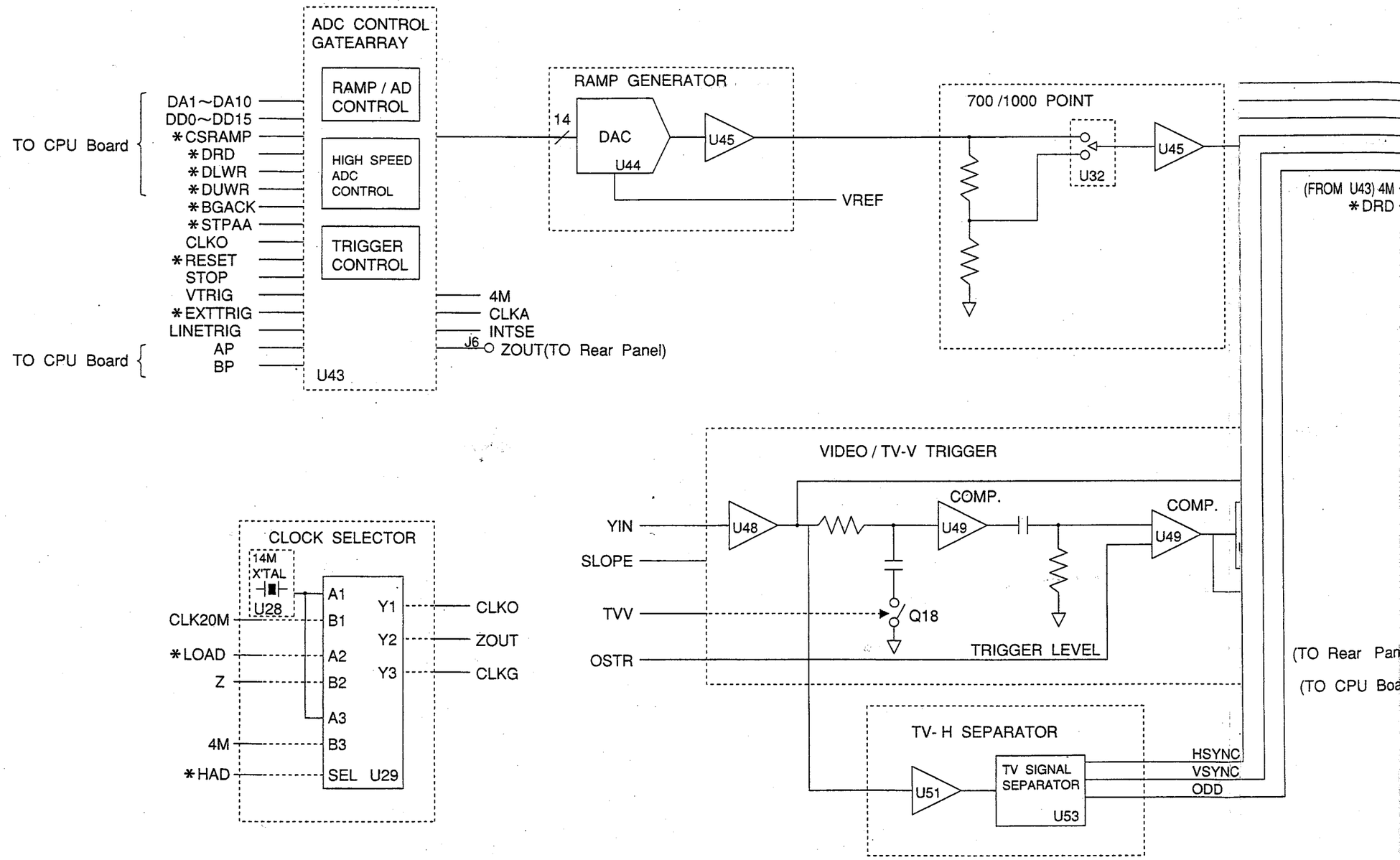
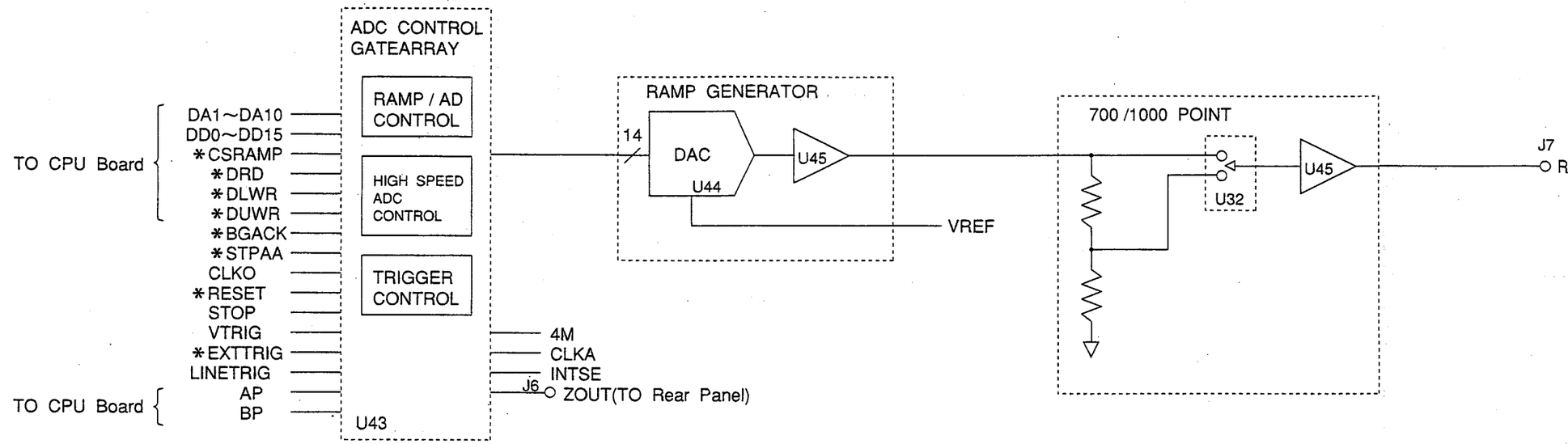
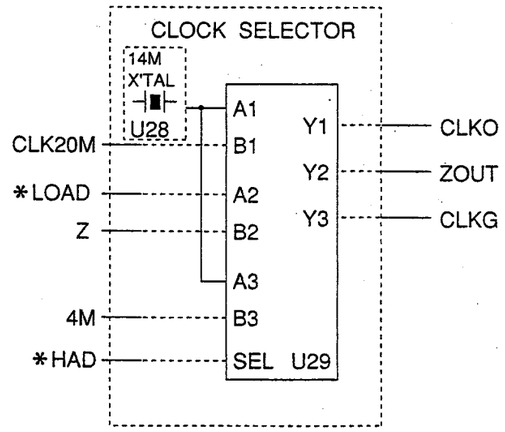
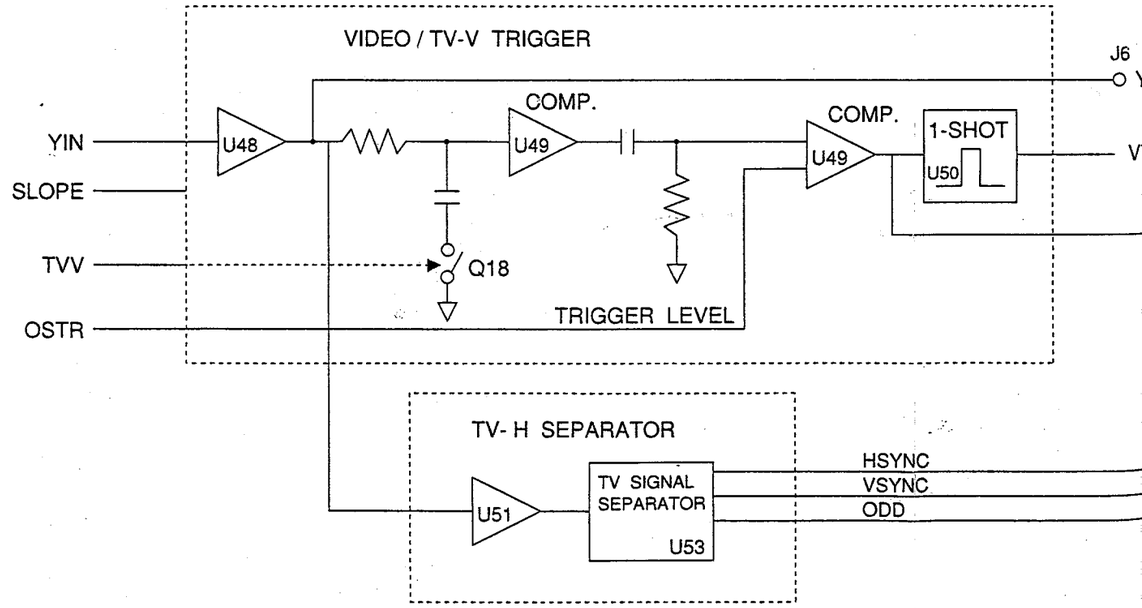


Figure 6-12 AD BLOCK DIAGRAM(1)


ADC CONTROL
GATEARRAY
RAMP / AD
CONTROL
HIGH SPEED
ADC
CONTROL
TRIGGER
CONTROL
U43
TO CPU Board
DA1~DA10
DD0~DD15
*CSRAMP
*DRD
*DLWR
*DUWR
*BGACK
*STPAA
CLKO
*RESET
STOP
VTRIG
*EXTTRIG
LINETRIG
TO CPU Board
AP
BP
4M
CLKA
INTSE
J6
ZOUT(TO Rear Panel)
RAMP GENERATOR
14
DAC
U44
U45
VREF
700 /1000 POINT
U32
U45
(FROM U43) 4M
*DRD
CLOCK SELECTOR
14M
X'TAL
U28
CLK20M
*LOAD
Z
4M
*HAD
A1
B1
A2
B2
A3
B3
SEL U29
Y1
Y2
Y3
CLKO
ZOUT
CLKG
VIDEO / TV-V TRIGGER
YIN
SLOPE
TVV
OSTR
U48
COMP.
U49
COMP.
U49
Q18
TRIGGER LEVEL
(TO Rear Pan
(TO CPU Boa
TV- H SEPARATOR
U51
TV SIGNAL
SEPARATOR
U53
HSYNC
VSYNC
ODD


ADC CONTROL
GATEARRAY
RAMP / AD
CONTROL
HIGH SPEED
ADC
CONTROL
TRIGGER
CONTROL
U43
TO CPU Board
DA1~DA10
DD0~DD15
*CSRAMP
*DRD
*DLWR
*DUWR
*BGACK
*STPAA
CLKO
*RESET
STOP
VTRIG
*EXTTRIG
LINETRIG
TO CPU Board
AP
BP
4M
CLKA
INTSE
J6
ZOUT(TO Rear Panel)
RAMP GENERATOR
14
DAC
U44
U45
VREF
700 /1000 POINT
U32
U45
J7
R


CLOCK SELECTOR
14M
X'TAL
U28
CLK20M
*LOAD
Z
4M
*HAD
A1
B1
A2
B2
A3
B3
SEL
Y1
Y2
Y3
U29
CLKO
ZOUT
CLKG


VIDEO / TV-V TRIGGER
YIN
SLOPE
TVV
OSTR
U48
COMP.
U49
COMP.
U49
1-SHOT
U50
Q18
TRIGGER LEVEL
J6
V
TV- H SEPARATOR
U51
TV SIGNAL
SEPARATOR
U53
HSYNC
VSYNC
ODD

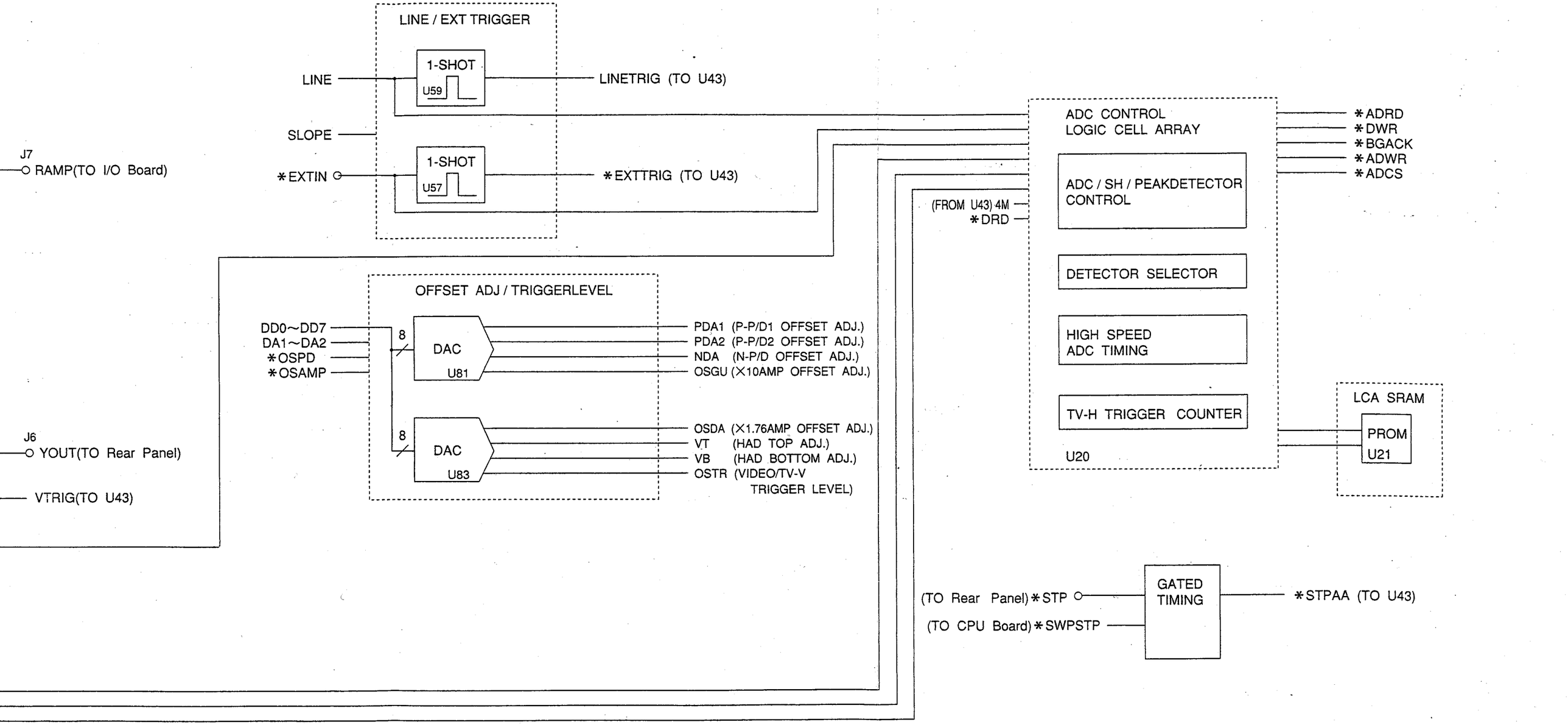


Figure 6-13 AD BLOCK DIAGRAM(2)

6.6 CPU Section

(1) Turn the power switch on. If the screen does not light and if the power supply is normal, the CRT display itself has failed or the signal cable between the CPU board and CRT display has failed. Otherwise, the CPU board itself has failed.

(2) Check the ROM's. If one of them has failed, its error message given below may be output:
"ROM #1 (upper) is error!!"
"ROM #1 (lower) is error!!"
"ROM #2 (upper) is error!!"
"ROM #2 (lower) is error!!"
The ROM chip has failed. Replace the U28, U29, U30, or U31 with a new one.

(3) Check the RAM's. If one of them has failed, its error message given below may be output:
"CPU RAM (xxxx) is error!!", xxxx
"BKUP RAM (xxxx) is error!!", xxxx
"BIT RAM (xxxx) is error!!", xxxx
The RAM chip has failed. Replace the RAM board with a new one.

CAUTION

If the fault board is replaced, the EEPROM data is changed. All system adjustment must be repeated again.

6.7 RF I/O Section

6.7.1 START And MULTIBAND OFFSET DAC

The START And MULTIBAND OFFSET DAC operates only when two or more bands of CENTER FREQUENCY, START, and STOP setup modes or SPAN setup mode are selected during frequency setup.

(1) Press the [PRESET] key of the R3265/3271 first, then press the [CENTER FREQ], [1], [GHz], [FREQ SPAN], [2] and [GHz] keys in this sequence.

(2) Connect the positive lead of DVM to pin 1 of U2, and connect the negative lead of DVM to TP5 (GV). Make sure that the signal voltage at DVM is −5V.

(3) Press the [START], [0] and [GHz] keys in this sequence, and make sure that the voltage at DVM is −10V.

(4) If the measured voltages differ from those given in Steps ① and ③, press the [MENU], [SWEEP MODE] and [MANUAL SWP] keys first, then press the [SHIFT], [BK SP], [ADDRESS &DATA], [4], [0], [0], [1], [0], [0], [Hz] and [WRITE ONLY] keys in this sequence to check the following:

① +10V must appear at pin 15 of U3.

② +5V must appear at pin 14 of U3.

③ TTL negative pulses must be output when pins 9 (WR) and 8 (CS) of U3 are monitored on the oscilloscope and the data knob is being set on the front panel.

(5) If the signal voltage is abnormal at pin 8 (CS) of U3, check the U54 (74HC138).

6.7.2 SPAN ATTENUATOR DAC

The SPAN ATTENUATOR DAC is used to attenuate sweep signals according to the specified span. The signal level can be controlled from approximately 1/1 to 1/20.

(1) Press the [PRESET] key of R3265/3271 first, then press the [CENTER FREQ], [1], [GHz], [FREQ SPAN], [2] and [GHz] keys in this sequence.

(2) To select the MANUAL SWEEP mode, press the [MENU], [SWEEP MODE] and [MANUAL SWP] keys in this sequence.

(3) Connect the positive lead of DVM to pin 1 of U5, and connect the negative lead of DVM to TP5 (GV).

(4) Adjust the data knob on the front panel so that the sweep marker comes to its start position. Also, make sure that +2.44V appear at the DVM.

(5) If this value is abnormal, check the following:

① −5V must appear at pin 15 of U4.

② Press the [SPAN] key.

The TTL negative pulses must appear at pins 9 (WR) and 8 of U4 on the oscilloscope when the data knob is being adjusted.

(6) If the signal voltage is abnormal at pin 8 (CS) of U4, check the U53 (74HC138).

6.7.3 SPAN ADJUSTMENT DAC

The SPAN ADJUSTMENT DAC is used to adjust the span accuracy and it has approximately 10% of adjustable range.

(1) Press the [PRESET] key of R3265/3271 first, then press the [CENTER FREQ], [1], [GHz], [FREQ SPAN], [2] and [GHz] keys in this sequence.

(2) To select the MANUAL SWEEP mode, press the [MENU], [SWEEP MODE] and [MANUAL SWP] keys in this sequence.

(3) Connect the positive lead of DVM to pin 1 of U6, and connect the negative lead of DVM to TP5 (GV).

(4) Adjust the data knob on the front panel so that the sweep marker comes to its start position.

(5) Press the [SHIFT], [BK SP], [ADDRESS &DATA], [4], [0], [0], [1], [1], [0], [Hz] and [WRITE ONLY] keys in this sequence. Adjust the data knob on the front panel to change data between "00" and "ff". Then, make sure that the DVM measured value can be set between 0V and approximately −2.4V when the data is changed between "00" and "ff".

(6) If the measured value is abnormal, check the following:

① Approximately +2.4V must appear at pin 4 of U7.

② The TTL negative pulses must appear at pins 15 (CS) and 16 (WR) of U7 on the oscilloscope when the data knob is being adjusted.

(7) If the signal voltage is abnormal at pin 15 (CS) of U7, check the U54 (74HC138).

6.7.4 Span Control Switches

The LOG SPAN and LIN SPAN can be set during span adjustment. The YTO main coil, FM coil, and VCO signals are sweeped under control of analog switches U8, U10, U16, U17, and U18 (DG201).

(1) Table 6-26 lists the span switch setup.

Table 6-26 LIN SPAN

SPAN \ Pin No.	U10				U16				U17				U18	
	1	8	9	16	1	8	9	16	1	8	9	16	8	9
4.01 GHz to	L	L	H	H	L	L	H	L	H	H	L	H	H	L
401 MHz to 4 GHz	L	L	H	H	L	L	H	H	H	H	L	H	H	L
40.1 MHz to 400 MHz	L	L	H	H	L	L	H	H	L	H	L	H	H	L
10.1 MHz to 40 MHz	L	L	H	H	L	L	H	H	H	H	L	L	H	L
2.01 MHz to 10 MHz	L	L	H	H	H	H	L	H	H	H	L	H	L	H
to 2 MHz	L	L	H	H	H	H	L	H	H	L	H	H	H	L
0 MHz	L	L	H	H	H	H	L	H	H	H	L	H	H	L

(2) The LOG SPAN can be set as follows:

① The signal at pin 8 of U10 is set to high but the signal at pin 9 is set to low.

② Table 6-27 lists the U8 signal setup.

Table 6-27 LOG SPAN

STOP FREQ: START FREQ	U8 Pin No.			
	1	8	9	16
10:1	H	–	L	H
100:1	H	–	H	L
1000:1	L	–	H	H

③ U16, U17 and U18 can be set in the same way as when the STOP FREQ of LOG SPAN is set according to the SPAN of Table 6-26.

6.7.5 LOG SPAN OFFSET DAC

The LOG SPAN OFFSET DAC is the D/A converter for offset voltage adjustment of the Unti Log circuit consisting of U9 and Q6 of the LOG SPAN circuit. The DAC is controlled between "00" and "ff" of data sent from the CPU board.

(1) Press the [PRESET] key of R3265/3271. Then, select the SINGLE SWEEP mode by pressing the [MENU], [SWEEP MODE] and [SINGLE SWP] keys in this sequence.

(2) Connect the positive lead of DVM to pin 7 of U6, and connect the negative lead of it to TP5 (GV).

(3) Press the [SHIFT], [BK SP], [ADDRESS], [4], [0], [0], [1], [1], [2] and [Hz] keys in this sequence. Then, press the [WRITE ONLY] key and adjust the data control to change data from "00" tp "ff". If the measured DVM value does not change to 0V to −10V, check the following:

① +10V must appear at pin 18 of U7.

② +5V must appear at pin 17 of U7.

③ TTL negative pulses must appear at pins 16 (WR) and 15 (CS) of U7 when monitored on the oscilloscope and the data knob is being set on the front panel.

(4) If the signal at pin 15 (CS) of U7 is abnormal in Substep ③ of Step (3), check the U54 (74HC138)

6.7.6 1/N ATTENUATOR DAC

The 1/N ATTENUATOR DAC is used for "1/n" signal attenuation in Harmonic Mixing Mode N when the high-band mixer of the R3271 is used. When the R3265 is used, all Band N values is equal to 1 and the attenuation is fixed to 4000 divided by 4095.

(1) Press the [PRESET] key of R3265/3271 first, then press the [CENTER FREQ], [1], [GHz], [FREQ SPAN], [2] and [GHz] keys in this sequence.

(2) To select the MANUAL SWEEP mode, press the [MENU], [SWEEP MODE] and [MANUAL SWP] keys in this sequence on the R3265/3271.

Also, adjust the data knob to set the sweep marker to its start position.

(3) Connect the positive lead of DVM to pin 1 of U11, and connect the negative lead of it to TP5 (GV). Make sure that the measured value at DVM is equal to the value of each center frequency defined on Table 6-28.

Table 6-28 Measured Values of DVM

CENTER FREQ.	Measured Value of DVM	N
2 GHz	−1.94 V	1
6 GHz	−1.94 V	1
10 GHz	−0.97 V	2
18 GHz	−0.65 V	3
25 GHz	−0.47 V	4

(4) If the measured value at DVM does not match the definition of Table 6-28, press the [SHIFT], [BK SP], [ADDRESS &DATA], [4], [0], [0], [0], [1], [0], [Hz] and [WRITE ONLY] keys in this sequence on the R3265/3271. Check the following:

① +2.0V must appear at pin 15 of U12.

② +5V must appear at pins 13 and 14 of U12.

③ TTL negative pulses must appear at pins 8 (CS) and 9 (WR) of U12 when monitored on the oscilloscope and the data knob is being set on the front panel.

(5) If the signal voltage is abnormal at pin 8 (CS) of U12, check the U53 (74HC138).

6.7.7 YTO MAIN COIL TUNE DAC

The YTO MAIN COIL TUNE DAC is the D/A converter and used for determination of current of the YIG oscillator. It is controlled by the CENTER FREQ setup.

(1) Press the [PRESET] key on the R3265/3271 first, then press the [CENTER FREQ], [0], [MHz], [FREQ SPAN], [0] and [MHz] keys in this sequence.

(2) Connect the positive lead of DVM to pin 6 of U20, and connect the negative lead of it to TP15 (GV). Make sure that the measured voltage at DVM is −0.88V.
Then, press the [CENTER FREQ], [3], [.], [6] and [GHz] keys in this sequence to be sure the measured value at DVM is −9.67V.

(3) If the measured value at DVM differs from this definition, press the [MENU], [SWEEP MODE] and [SINGLE SWP] keys in this sequence and check the following:
① +10V must appear at pin 15 of U19.
② +5V must appear at pins 13 and 14 of U19.
③ TTL negative pulses must appear at pins 8 (CS) and 9 (WR) of U19 when monitored on the oscilloscope and the data knob is being set on the front panel.

(4) If the signal voltage is abnormal at pin 8 (CS) of U19, check the U53 (74HC138).

6.7.8 3.5 GHz TUNE ADJUSTMENT DAC

The 3.5 GHz TUNE ADJUSTMENT DAC is the D/A converter and used for adjustment of current variation of the YTO MAIN COIL TUNE DAC. The main coil tuning voltage can be attenuated.

(1) Press the [PRESET] key of the R3265/3271 first, then press the [CENTER FREQ], [3], [.], [5], [GHz], [FREQ SPAN], [0] and [MHz] keys in this sequence.
Press the [MENU], [SWEEP MODE] and [SINGLE SWP] keys in this sequence.
Then, press the [SHIFT], [BK SP], [ADDRESS &DATA], [4], [0], [0], [1], [2], [0], [Hz] and [WRITE ONLY] keys in this sequence.

(2) Connect the positive lead of DVM to pin 1 of U22, and connect the negative lead of it to TP15 (GV).

(3) Make sure that the measured value at DVM changes from 0V to +9.42V when the data is changed from "00" to "ff" using the data knob on the front panel.

(4) If the measured value at DVM does not change, check the following:

① −9.42V must appear at pin 4 of U21.

② TTL negative pulses must appear at pins 15 (CS) and 16 (WR) of U21 when monitored on the oscilloscope and the data is being changed by the data knob on the front panel.

If the signal voltage is abnormal at pin 15 (CS) of U21, check the U54 (74HC138).

6.7.9 0 GHz ADJUSTMENT DAC

The 0 GHz ADJUSTMENT DAC is the D/A converter which adjusts the YTO frequency to 4231 MHz when the CENTER FREQ is set to 0 MHz.

(1) Press the [PRESET] key of the R3265/3271 first, then press the [CENTER FREQ], [0], [MHz], [MENU], [SWEEP MODE] and [SINGLE SWP] keys in this sequence.

(2) Press the [SHIFT], [BK SP], [ADDRESS &DATA], [4], [0], [0], [1], [2], [2], [Hz] and [WRITE ONLY] keys in this sequence.

(3) Connect the positive lead of DVM to pin 7 of U22, and connect the negative lead of it to TP15 (GV).

Make sure that the measured value at DVM changes from 0V to −10V when the data is changed from "00" to "ff" using the data knob on the front panel.

(4) If the measured value at DVM does not change, check the following:

① +10V must appear at pin 18 of U21.

② +5V must appear at pin 17 of U21.

③ TTL negative pulses must appear at pins 15 (CS) and 16 (WR) of U21 when monitored on the oscilloscope and the data is being set by the data knob on the front panel.

(5) If the signal voltage is abnormal at pin 15 (CS) of U21, check the U54 (74HC138).

6.7.10 YTO Main Coil Filter Driver

If the SPAN has been set to below 10 MHz, the YTO is set in the FM Coil Sweep mode. Insert the capacitance across the coil to reduce the current noise of the main coil.

(1) Press the [PRESET] key of the R3265/3271, and set as follows: [CENTER FREQ] [0] [MHz] and [FREQ SPAN] [1] [0] [MHz].

(2) Connect the positive lead of DVM to the collector of Q7, and connect the negative lead to TP15 (GV). Also, make sure that the voltage at DVM is approximately 0V.

(3) Set [FREQ SPAN] [1] [1] [MHz], and make sure that the voltage at DVM is +15V.

(4) If not, perform the following substeps:

① Make sure that the signal at pin 5 of U63 is TTL high if FREQ SPAN is 10 MHz.

② Make sure that the signal at pin 5 of U63 is TTL low if FREQ SPAN is 11 MHz.

(5) If the signal at pin 5 of U63 is abnormal, press the [MENU], [SWEEP MODE] and [SINGLE SWP] keys in this sequence on the R3265/3271 to select the SINGLE SWEEP mode. Then, set [SHIFT] [BK SP] [ADDRESS &DATA] [4] [0] [0] [0] [5] [0] [Hz] and monitor the signal at pin 3 of U63 on an oscilloscope.

Make sure that TTL negative pulses appear when the data knob is used on the front panel.

(6) If the pulses are not output, check the U53 (74HC138).

6.7.11 YTO PLL Circuit

The error voltage of the YTO PLL (Phase-Locked Loop) is entered in J8. Accurately set the first local frequency by controlling the YTO FM Coil current.

(1) Press the [PRESET] key on the R3265/3271, and set as follows: [CENTER FREQ] [1] [GHz] and [FREQ SPAN] [5] [0] [0] [MHz].

(2) Monitor signals at pins 16 and 1 of U18 on the DVM or oscilloscope.

Make sure that they have the signal levels as defined on Table 6-29 when the span is. adjusted.

Table 6-29 YTO PLL Control

SPAN	U18	
	Pin1	Pin16
500 MHz	H	L
501 MHz	L	H

(3) If the signal levels are incorrect, perform the following substeps:

① Press the [MENU], [SWEEP MODE] and [SINGLE SWP] keys in this sequence to select the SINGLE SWEEP mode.

Then, follows: [SHIFT] [BK SP] [ADDRESS &DATA] [4] [0] [0] [0] [4] [0] [Hz] [WRITE ONLY].

② Monitor the signal at pin 19 of U61 on an oscilloscope, and make sure that TTL negative pulses appear when the data knob is used on the front panel.

(4) If the pulses are abnormal, check the U53 (74HC138).

6.7.12 RF Bias Control DAC

The RF Bias Control DAC is an 8-bit Quad D/A converter that controls the EXT MIX Bias, Harmonic MIX Bias (R3271 only), and Band Gain.

(1) Press the [PRESET] key on the R3265/3271, and set as follows: [MENU] [SWEEP MODE] [SINGLE SWP] in this sequence to select the SINGLE SWEEP mode.

(2) Check the Harmonic MIX Bias Adjustment D/A Converter as follows:

① Press the [SHIFT] [BK SP] [ADDRESS &DATA] [4] [0] [0] [1] [3] [0] [Hz] [WRITE ONLY].

② Connect the positive lead of DVM to pin 1 of U32, and connect the negative lead to TP15 (GV). Make sure that the voltage changes from 0 to 10V on the DVM when data is changed from "00" to "ff" with the data knob of the front panel.

(3) Check the EXT MIX Bias Adjustment DAC in the following procedure:

① Set as follows: [SHIFT] [BK SP] [ADDRESS &DATA] [4] [0] [0] [1] [3] [2] [Hz] [WRITE ONLY].

② Connect the positive lead of DVM to pin 2 of U32, and connect the negative lead to TP15 (GV). Make sure that the voltage changes from 0 to 10V on the DVM when data is changed from "00" to "ff" with the data knob of the front panel.

(4) Check the Band Gain Control DAC as follows:

① Set as follows: [SHIFT] [BK SP] [ADDRESS &DATA] [4] [0] [0] [1] [3] [4] [Hz] [WRITE ONLY].

② Connect the positive lead of DVM to pin 20 of U32, and connect the negative lead to TP15 (GV). Make sure that the voltage changes from 0 to 10V on the DVM when data is changed from "00" to "ff" with the data knob of the front panel.

③ Set as follows: [SHIFT] [BK SP] [ADDRESS &DATA] [4] [0] [0] [1] [3] [6] [Hz] [WRITE ONLY].
Connect the positive lead of DVM to pin 19 of U32. Make sure that the voltage changes from 0 to 10V on the DVM when data is changed from "00" to "ff" with the data knob of the front panel.

(5) If the value measured on the DVM does not change in Steps (2) to (4), check the following:

① Make sure that 10V appear at pin 4 of U32.

② Make sure the TTL negative pulses appear at pin 15 of U32 when it is monitored on the oscilloscope and when the data knobs are used on the front panel.

(6) If these pulses are not output at pin 15 (C5) of U32, check the V54 (74HC138).

6.7.13 Slope Gain DAC

The Slope Gain DAC is a D/A converter for compensation of the frequency response of each signal band. The YTO Drive voltage is attenuated and used for this DAC.

(1) Press the [PRESET] key on the R3265/3271, and set as follows: [START] [0] [MHz] , [STOP] [3] [.] [6] [GHz] .
Then, press the [MENU] , [SWEEP MODE] and [MANUAL SWP] keys in this sequence.
Adjust the sweep marker to locate on the stop line by using the data knob of the front panel.

(2) Set as follows: [SHIFT] [BK SP] [ADDRESS &DATA] [4] [0] [0] [1] [4] [2] [Hz] [WRITE ONLY] .
Connect the positive lead of DVM to pin 7 of U36, and connect the negative lead to TP15 (GV).
Make sure that the voltage changes from 0 to approximately −5.5V on the DVM when data is changed from "00" to "ff" with the data knob of the front panel.

(3) If an invalid value is obtained in Step (2), check the following:
① Make sure that approximately +5.5V appear at pin 18 of U37.
② Make sure that −15V appear at pin 17 of U37.
③ Make sure that TTL negative pulses appear at pins 15 (CS) and 16 (WR) of U37 when monitored on the oscilloscope and when the data knob is adjusted on the front panel.

(4) If an invalid signals appear at pin 15 (C5), check the U54 (74HC138).

6.7.14 Band Control Circuits

The Band Control Circuits generate signals so that the third converter selects an input when each of Base Band Mixer, High-Band Mixer, and EXT Mixer has been set.

(1) Press the [PRESET] key on the R3265/3271, and set as follows: [CENTER FREQ] [1] [GHz] , [FREQ SPAN] [1] [GHz] .

(2) Press the [MENU] [SWEEP MODE] [MANUAL SWP] keys in this sequence.
Check signals at pins 1, 7, 8, and 14 of U31 using the DVM, and make sure that these signals are the same as those defined on Table 6-30 when the center frequency is changed.
It is assumed that the EXT Mixer band has been set to [CENTER FREQ] and [EXT MIX] .

Table 6-30 Band Control (1)

CENTER FREQ (GHz)	U31			
	Pin1	Pin7	Pin8	Pin14
1	−14 V	−14 V	−14 V	+14 V
5	+14 V	−14 V	+14 V	−14 V
EXT MIX	−14 V	+14 V	−14 V	−14 V

(3) If the voltages at each pin of U31 do not match the values of Table 6-30, check the followings:

① Make sure that signals at pins 2, 6, 9, and 13 of U31 match those defined on Table 6-31.

Table 6-31 Band Control (2)

CENTER FREQ (GHz)	U31			
	Pin2	Pin6	Pin9	Pin13
1	H	H	H	L
5	L	H	L	H
EXT MIX	H	L	H	H

② Make sure that the voltage at pin 3 of U31 is +2.3V.

(4) If these voltages are incorrect (not equal to +2.3V), check the U60.

(5) If they are correct, set as follows: SHIFT, BK SP, ADDRESS &DATA, 4, 0, 0, 2, 1, 0, Hz, WRITE ONLY.

Monitor the signal at pin 45 of U55 on the oscilloscope.

Make sure that the TTL negative pulses appear when the data knob is adjusted on the front panel.

(6) If these pulses are incorrect at pin 45 of U55, check the U52 (74HC138).

6.7.15 YTF Gain Adjustment DAC

The preselector (YTF) is inserted in the high-band input (3.5 GHz or more) of the R3265/3271. The YTF Gain Adjustment D/A Converter is used to adjust the YTF timing sensitivity.

(1) Press the [PRESET] key on the R3265/3271, and set as follows: [CENTER FREQ] [7] [.] [5] [GHz] , [FREQ SPAN] [0] [MHz] .
Then, press the [MENU] [SWEEP MODE] and [SINGLE SWP] keys in this sequence to select the SINGLE SWEEP mode.

(2) Set as follows: [SHIFT] [BK SP] [ADDRESS &DATA] [4] [0] [0] [1] [4] [0] [Hz] [WRITE ONLY] .
Connect the positive lead of the DVM to pin 1 of U68, and connect the negative lead to TP15 (GV).
Make sure that the voltage measured on the DVM changes from 0 to approximately −8.3V when data is changed from "00" to "ff" using the data knob of the front panel.

(3) If the voltage is incorrect, check the following:
① Approx. +8.3V must appear at pin 4 of U37.
② +5V must appear at pin 17 of U37.
③ TTL negative pulses must appear at pins 16 (WR) and 15 (CS) of U37 when they are monitored on the oscilloscope and when data is set using the data knob of the front panel.

(4) If the voltage is incorrect at pin 15 (CS) of U37, check the U54 (74HC138).

6.7.16 YTF Offset Adjustment DAC

The YTF Offset Adjustment D/A Converter adjusts the YTF tuning offset of the YTF Offset Adjustment DAC. It consists of the coarse and fine adjustment DAC sections.

(1) Press the [PRESET] key on the R3265/3271, and set as follows: [MENU] [SWEEP MODE] and [SINGLE SWP].

(2) Check the Coarse Offset Adjustment DAC as follows:

① Set as follows: [SHIFT] [BK SP] [ADDRESS &DATA] [4] [0] [0] [1] [5] [0] [Hz] [WRITE ONLY].

② Connect the positive lead of the DVM to pin 1 of U43, and connect the negative lead to TP15 (GV).

Make sure that the voltage measured on the DVM changes from 0 to approximately −10V when data is changed from "00" to "ff" using the data knob of the front panel.

(3) Check the Fine Offset Adjustment DAC as follows:

① Set as follows: [SHIFT] [BK SP] [ADDRESS &DATA] [4] [0] [0] [1] [5] [2] [Hz] [WRITE ONLY].

② Connect the positive lead of the DVM to pin 7 of U43, and make sure that the voltage measured on the DVM changes from 0 to −10V when data is changed "00" to "ff" using the data knob of the front panel.

(4) If the voltage is incorrect, check the following 3 points:

① +10V must appear at pin 4 of U42.

② +5V must appear at pin 17 of U42.

③ TTL negative pulses must appear at pins 16 (WR) and 15 (CS) of U42 when they are monitored on the oscilloscope and when data is set using the data knob of the front panel.

(5) If the pulses are incorrect at pin 15 (CS) of U42 check the U52 (74HC138).

6.7.17 YTF Band Control Switches

The YTF sweep signals are multiplied by N-times for the High-Band MIX band of the R3271. Also, the R3265 uses value N = 1 for the 7.5 to 8 GHz band, and the 842 MHz YTF tuning frequency is controlled to be increased. They are executed by the U38 and U39 analog switches.

(1) Press the [PRESET] key on the R3265/3271, and set as follows: [CENTER FREQ] [0] [GHz], [FREQ SPAN] [0] [MHz].
Then, press the [MENU] [SWEEP MODE] and [SINGLE SWP] keys in this sequence.

(2) Change the center frequency and make sure that the control input of U38 and U39 switches matches the one defined on Table 6-32.

Table 6-32 YTF Band Control

R3271 ONLY

CENTER FREQ (GHz)	U38				U39	
	Pin1	Pin8	Pin9	Pin16	Pin8	Pin9
0 5	H H	H H	H H	H L	H H	L H
10	L	H	H	H	H	H
20 25	H H	H L	L H	H H	H H	H H

R3265 ONLY

CENTER FREQ (GHz)	U38				U39	
	Pin1	Pin8	Pin9	Pin16	Pin8	Pin9
0	H	H	H	H	H	L
5	H	L	H	H	H	H
8	H	L	H	H	L	H

(3) If incorrect, check the U60.

(4) If the U60 is normal, check the U55 as follows:

① Set as follows: [SHIFT] [BK SP] [ADDRESS &DATA] [4] [0] [0] [2] [1] [0] [Hz] [WRITE ONLY].
Make sure that TTL negative pulses appear at pins 43 (WR) and 45 (CS) of U55 when they are monitored on the oscilloscope and when data is changed using the data knob of the front panel.

② If the pulses are incorrect at pin 45 (CS) of U55, check the U52 (74HC138).

6.7.18 YTF Noise Filter Circuit

The YTF Noise Filter Circuit inserts a capacitance across the YTF tuning coil to reduce the tuning current noise of the YTF when the span frequency is 2 MHz or less.

(1) Press the [PRESET] key on the R3265/3271, and set as follows: [CENTER FREQ] [5] [GHz], [FREQ SPAN] [2] [MHz].

(2) Make sure that −15V appears at pin 2 of U69.

(3) Set as follows: [FREQ SPAN] [2] [.] [1] [MHz].
Make sure that the voltage is 0 V at pin 2 of U69.

(4) If the voltage is incorrect, make sure that the voltage at pin 2 of U67 is 0 V when the FREQ SPAN is 2 MHz and that the voltage is +5V when it is 2.1 MHz.

(5) If the voltage of U67 is incorrect, check the U58 and U55. Check the U55 as follows:

① Press the [MENU], [SWEEP MODE] and [SINGLE SWP] keys in this sequence to select the SINGLE SWEEP mode.
Then, set as follows: [SHIFT] [BK SP] [ADDRESS &DATA] [4] [0] [0] [2] [0] [0] [Hz] [WRITE ONLY].

② Make sure that TTL negative pulses appear at pins 43 (WR) and 45 (CS) of U55 when they are monitored on the oscilloscope and when data is changed using the data knob of the front panel.

③ If the pulses are incorrect at pin 45 (CS) of U55, check the U52 (74HC138).

6.7.19 Frequency Ref Adjustment DAC

The Frequency Ref Adjustment D/A Converter adjusts the 10 MHz Frequency Reference Oscillator, and the DAC output is sent to the STD Block (WBC-32xxSTD).

(1) Press the [PRESET] key on the R3265/3271, and set as follows: [MENU], [SWEEP MODE] and [SINGLE SWP].

(2) Set as follows: [SHIFT] [BK SP] [ADDRESS &DATA] [4] [0] [0] [1] [7] [2] [Hz] [WRITE ONLY].

(3) Connect the positive lead of the DVM to pin 7 of U72, and connect the negative lead to TP15 (GV).
Make sure that the voltage measured on the DVM changes from 0 to −10V when data is changed from "00" to "ff" using the data knob of the front panel.

(4) If the voltage measured on the DVM is incorrect, check the following:

① +10V must appear at pin 18 of U71,
② +5V must appear at pin 17 of U71,
③ TTL negative pulses must appear at pins 15 (CS) and 16 (WR) of U71 when they are monitored on the oscilloscope and when data is set using the data knob of the front panel.

(5) If the pulses are incorrect at pin 15 (CS) of U71, check the U54 (74HC138).

6.7.20 RF Attenuator Driver

The Input Attenuator is set for a combination of 10 dB, 20 dB and 40 dB on the R3265, and it is set for a combination of 10 dB, 20 dB, 20 dB and 20 dB on the R3271 within the range of 0 to 70 dB at every 10 dB.

(1) Press the [PRESET] key on the R3265/3271, and set as follows: [MENU] [SWEEP MODE] [SINGLE SWP].

(2) Press the [CPL] and [ATT] keys, and make sure that the inputs to U57 and U66 match the ones defined on Table 6-33 when the INPUT ATTENUATOR value is changed from 0 to 70 dB.

Table 6-33 Attenuator Setup

R3265 ONLY

ATTEN-UATOR (dB)	U57					
	Pin1	Pin2	Pin3	Pin4	Pin5	Pin6
0	L	H	L	H	L	H
10	H	L	L	H	L	H
20	L	H	H	L	L	H
30	H	L	H	L	L	H
40	L	H	L	H	H	L
50	H	L	L	H	H	L
60	L	H	H	L	H	L
70	H	L	H	L	H	L

R3271 ONLY

ATTEN-UATOR (dB)	U57						U66'	
	Pin1	Pin2	Pin3	Pin4	Pin5	Pin6	Pin6	Pin2
0	L	H	L	H	L	H	L	H
10	H	L	L	H	L	H	L	H
20	L	H	L	H	L	H	H	L
30	H	L	L	H	L	H	H	L
40	L	H	H	L	L	H	H	L
50	H	L	H	L	L	H	H	L
60	L	H	H	L	H	L	H	L
70	H	L	H	L	H	L	H	L

(3) If the attenuator setup is incorrect, check the following:

① Set as follows: [SHIFT] [BK SP] [ADDRESS &DATA] [4] [0] [0] [2] [4] [0] [Hz] [WRITE ONLY].

② Make sure that TTL negative pulses appear at pins 43 (WR) and 45 (CS) of U55 when they are monitored on the oscilloscope and when data is set using the data knob of the front panel.

(4) If the pulses are incorrect at pin 45 (CS) of U55, check the U52 (74HC138).

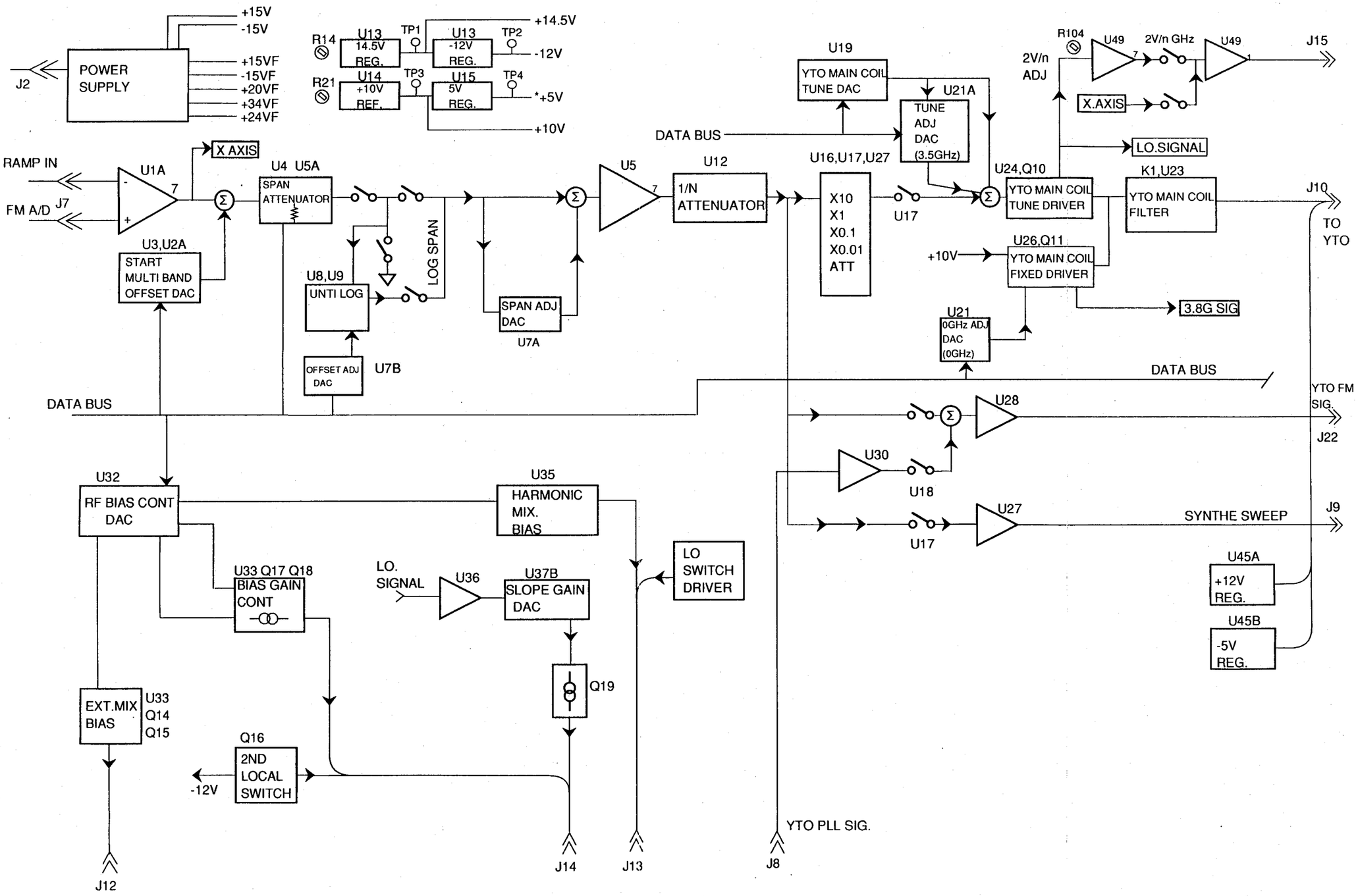


Figure 6-14 RF I/O BLOCK DIAGRAM(1)

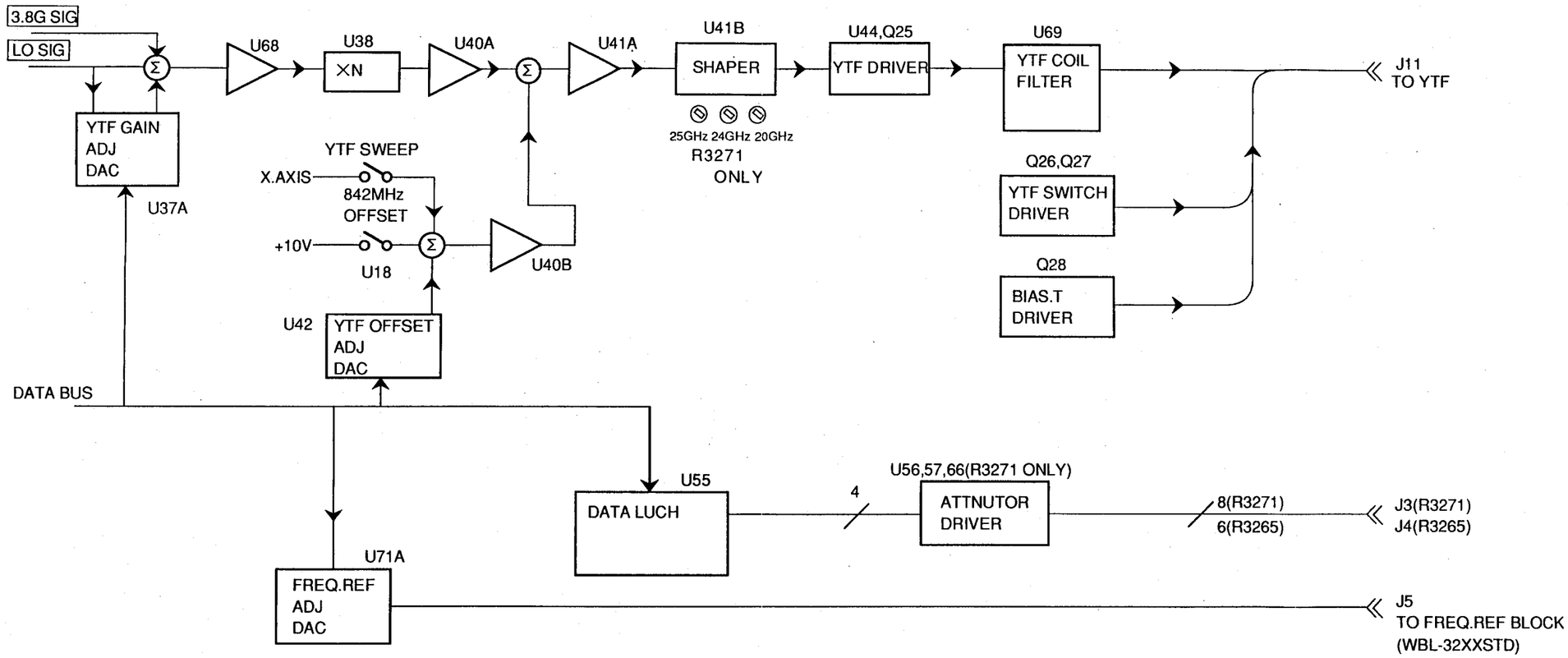


Figure 6-15 RF I/O BLOCK DIAGRAM(2)

6.8 Synthesizer Section

6.8.1 Before Synthesizer Troubleshooting

The Synthesizer has the following 4 PLL's:

- YTO PLL
- Sampler PLL
- VHF PLL (including R1 PLL, R2 PLL, and Offset PLL)
- Reference PLL

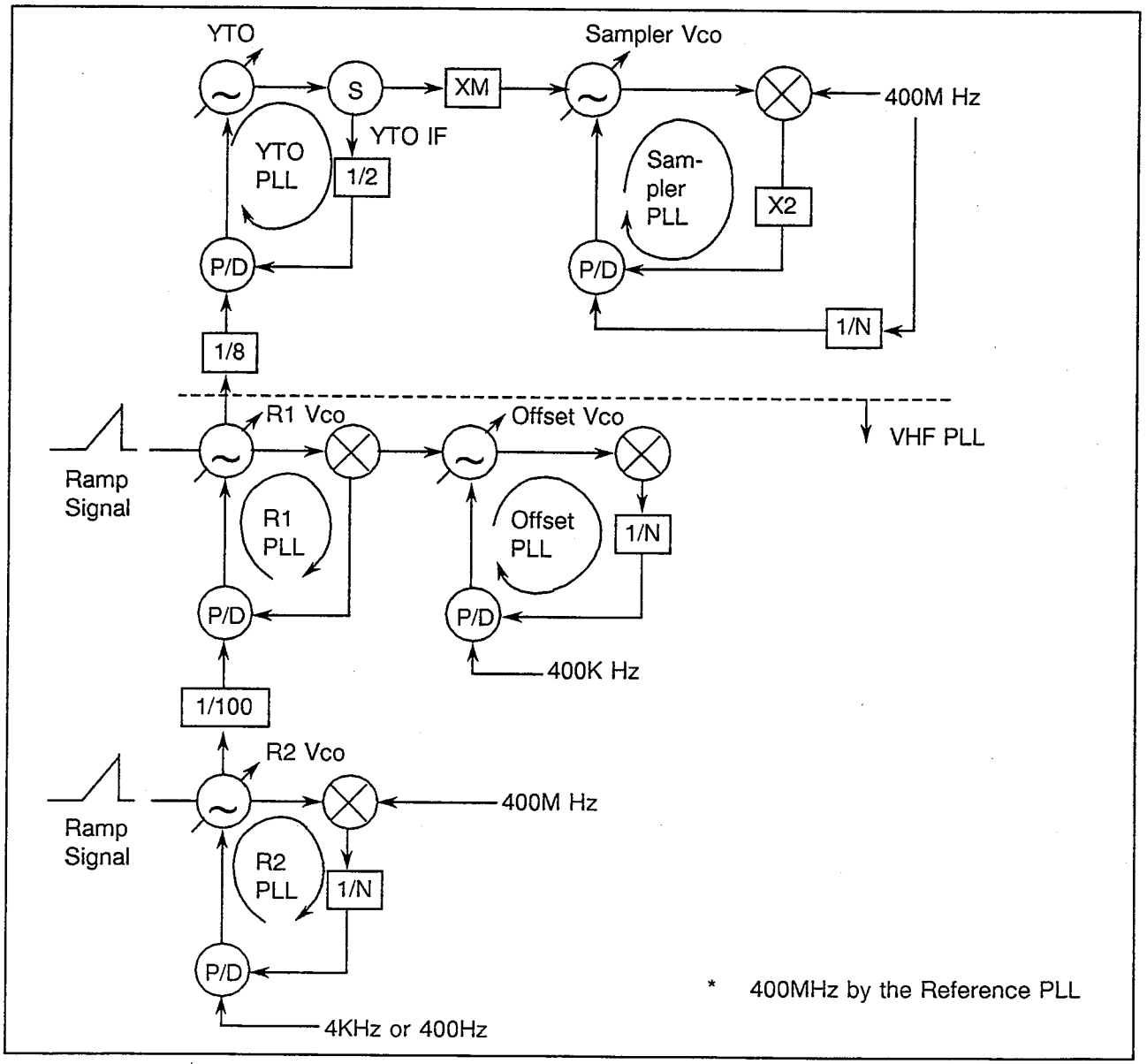
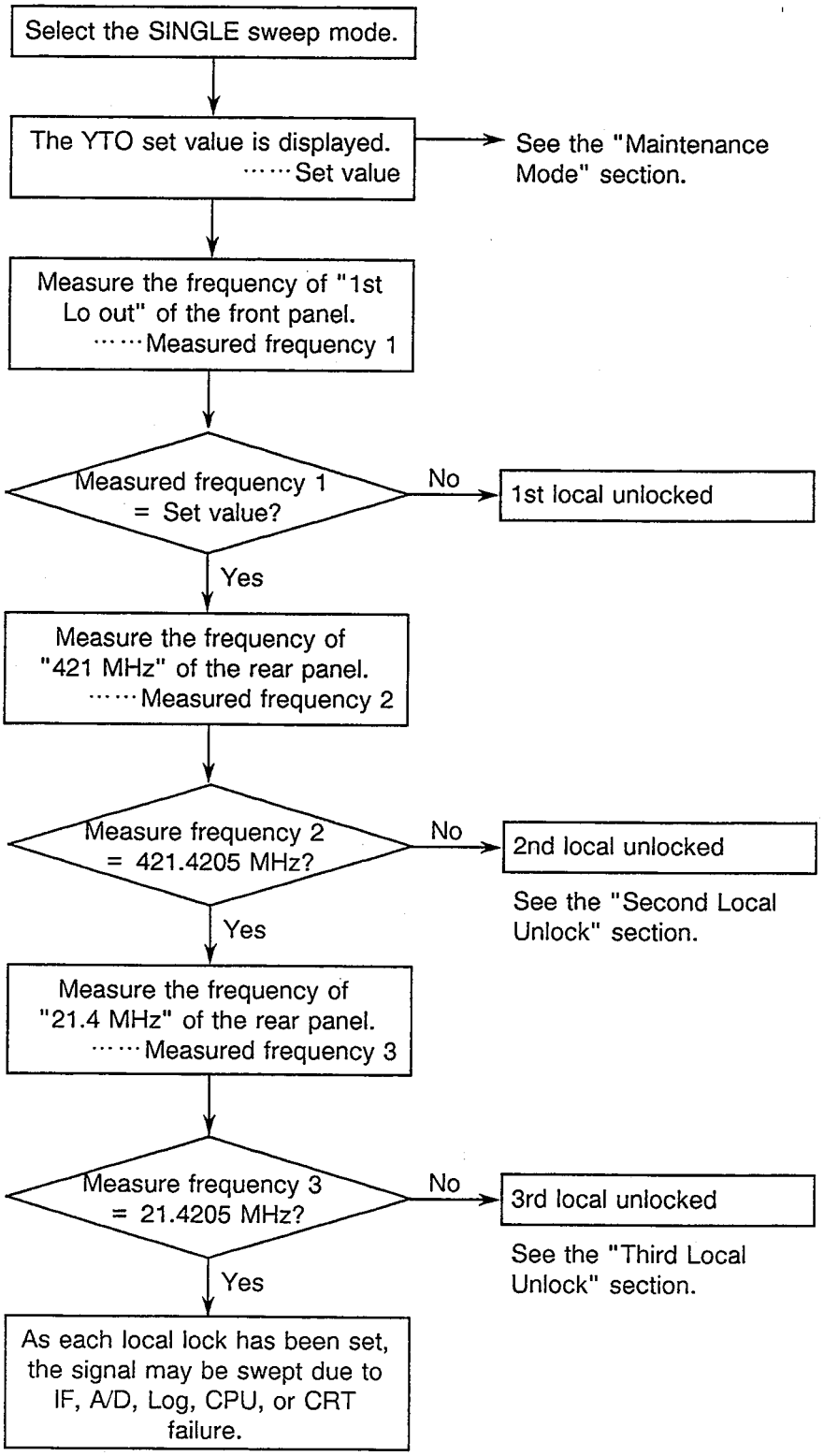


Figure 6-16 Synthesizer Block Diagram

Figure 6-16 shows the simple Synthesizer block diagram.
The Synthesizer generates the RF signals which are M times higher than the Sample VCO, and it generates the YTO IF signals. Also, the VHF PLL signals divided by 8 is used for YTO lock. The signals are swept by YTO, R1, and R2. They are switched by the signal span. The detailed block diagrams are shown in Figures 6-22 and 6-23, respectively.
The following describes the possible unlocked causes. They are:

- First local unlocked
- Second local unlocked
- Third local unlocked

Isolation procedure:



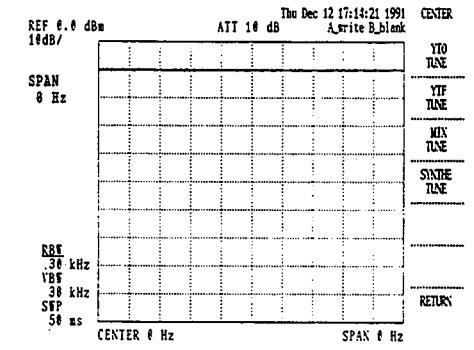
Notes during frequency measurement:

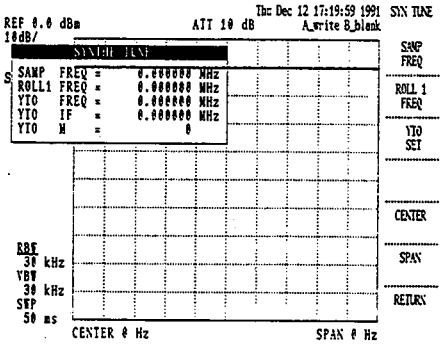
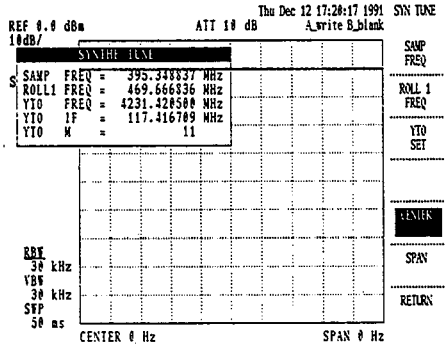
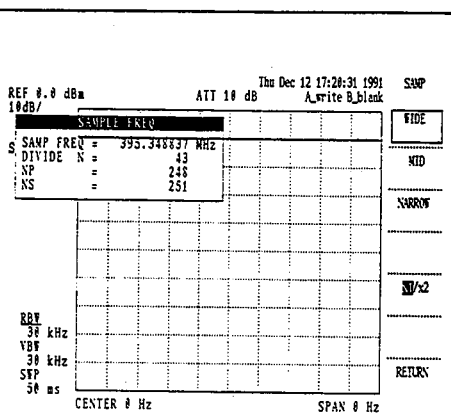
- Use a spectrum analyzer if it is available to use. This is because the YTO oscillation frequency may reach 8 GHz maximum.
- When using a spectrum analyzer or counter, synchronize the R3265/3271 with the 10 MHz reference frequency.
- Turn off the "CAL CORR" option of the Calibration menu as much as possible. This is because an error may occur between the set value and the measured value if this option is on. Each set value is assumed to be used when this option is off.

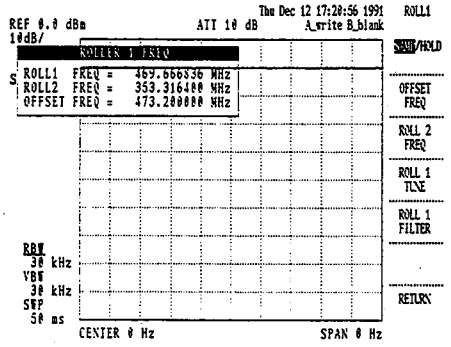
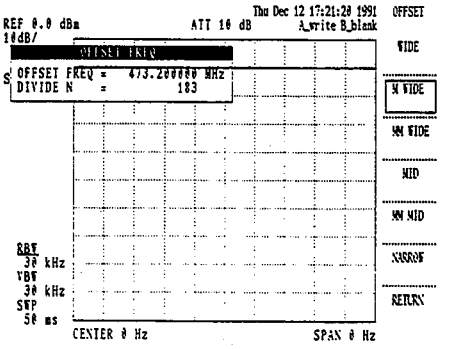
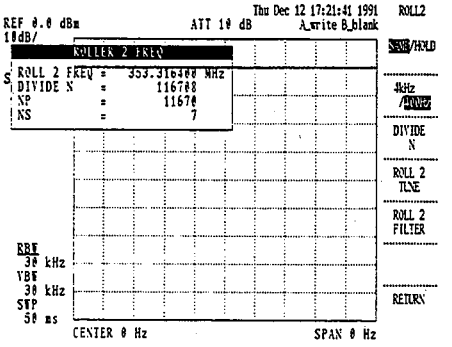
(1) Maintenance mode

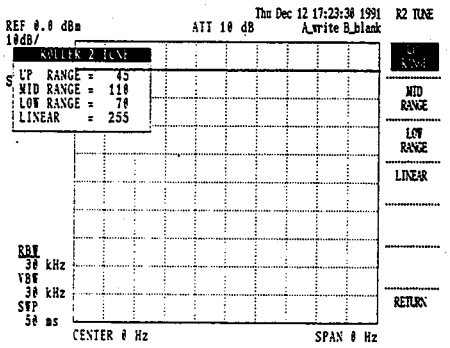
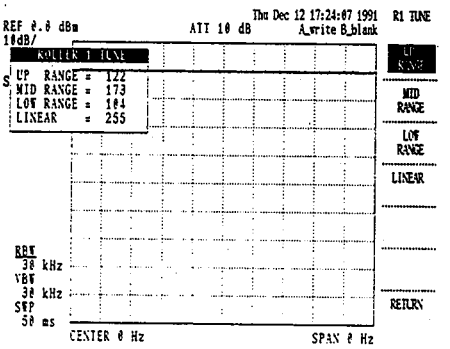
When starting the synthesizer troubleshooting, the user must select the Maintenance mode.
The following explains the Maintenance mode.
The Maintenance mode is selected only when the new version ROM has been installed.
To check it, hold down the [SHIFT] and press the [↑] key.
The ROM release date will be shown in the NOTE field of the screen. It must be July 9, 1991 or later.
The following explains the Maintenance mode of the Synthesizer Block.

Maintenance mode of Synthesizer Block:

Key Operation	Screen	Remarks
① [SHIFT] + [5] + [9] [4] [2] [8] [4]		The Maintenance mode is selected.

Key Operation	Screen	Remarks
② SYN THE TUNE software key		The Maintenance mode of the Synthesizer Block is selected.
③ CENTER software key + Desired center frequency		SAMP FREQ: Sampler PLL oscillation frequency ROLL1 FREQ: R1 PLL oscillation frequency YTO FREQ: YTO PLL oscillation frequency YTO IF: YTO IF frequency YTO M: Degree of sampler PLL radio frequency (Note: The set values during Cal Off)
④ SAMP FREQ software key		DIVIDE N: 400 MHz division ratio of sampler PLL Np: Divider set value (This value is converted into hexadecimal format and used as the set value of Address = 440220.) Ns: Divider set value (This value is converted into hexadecimal format and used as the set value of Address = 440260.)

Key Operation	Screen	Remarks
⑤ RETURN software key (to return to Step ③) ROLL 1 FREQ		ROLL2 FREQ: R2 PLL oscillation frequency OFFSET FREQ: Offset PLL oscillation frequency
⑥ OFFSET FREQ software key		DIVIDE N: Division ratio of offset PLL frequency
⑦ RETURN software key (to return to Step ⑤) ROLL 2 FREQ		DIVIDE N: Division ratio of R2 PLL frequency Np: Set value of address (440100 or 440140) Example: If Np = 11670 (decimal), it is "2a96" (HEX). The set value of address 440140 is "ff2d", and the set value of address 440100 is "ff96". Ns: Set value of address 440020 The set value is "ffx7". "x" is determined in the different condition.

Key Operation	Screen	Remarks
⑧ ROLL 2 TUNE software key		UP RANGE: Set value of R2 pretune DAC Ⓐ Address = 440320 MID RANGE: Set value of R2 pretune DAC Ⓑ Address = 4400E0 LOW RANGE: Set value of R2 pretune DAC Ⓒ Address = 4400C0 LINEAR: Set value of R2 lamp gain adjustment DAC Address = 440340 Note: The correction values must be added to the UP RANGE and LINEAR values and used as the set values.
⑨ RETURN RETURN software key (to return to Step ⑤) ROLL 1 FREQ		UP RANGE: Set value of R1 pretune DAC Ⓐ Address = 440330 MID RANGE: Set value of R1 pretune DAC Ⓑ Address = 4400A0 LOW RANGE: Set value of R1 pretune DAC Ⓒ Address = 440080 LINEAR: Set value of R1 lamp gain adjustment DAC Address = 440350 Note: The correction values must be added to the UP RANGE and LINEAR values and used as the set values.

To return to the Normal mode, repeat pressing the RETURN software key until the initial screen appears. In the Maintenance mode of the synthesizer, only the functions explained above are effective.

(2) Setup for first local troubleshooting

Before starting the troubleshooting of I/O board (BLL-017508X03), remove the screws from both the system and synthesizer board (BLS-017044, BLC-017046), and pull down the synthesizer board 90 degrees (see Figure 6-24).
Before starting the troubleshooting of synthesizer board:

① Remove all screws from the bottom cover where the I/O board exists.

② Remove the screws from the synthesizer board and set the board in the same status as shown in Figure 6-24.

③ Remove all screws from the synthesizer board at the top cover (where the I/O board exists) to allow easy troubleshooting of synthesizer board sides A and B.

CAUTION

Do not remove the screws from the top cover of the I/O and synthesizer boards. Also, do not remove the screws from the top cover of the synthesizer board attached to the system. This is because the I/O board has its GND terminal at the top cover of the synthesizer board.

(3) Notes during troubleshooting

① Handle the synthesizer and I/O board components with care as they may be damaged by the electrostatistics.

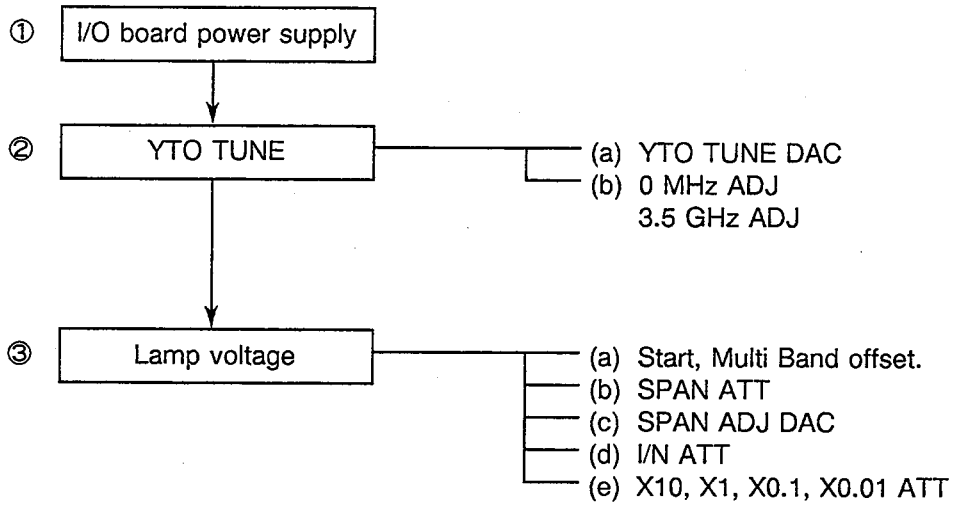
② Use the HP-54006A-6GHz probe or equivalent one to measure the signal level on the spectrum analyzer. If the HP-54006A-6GHz probe is used, the measured signal level is approx. 20 dBm less than the actual level.

③ All of the set values indicated in the Maintenance mode are obtained during Cal Off. (When the Maintenance mode is selected and the center value is set, the Cal Off set values are forcibly set for each synthesizer.) If the calibration is ON, the first local value is set so that the center shift of the 21.4 MHz IF filter is corrected. Therefore, this value may differ from the one indicated in the Maintenance mode.

6.8.2 Problems Due to Span

(1) Problems not associated with the span

The following explains the system when unlocked in all spans of all centers. The I/O board (BLL-017508X03) is also explained. The block diagram is shown in Figure 6-23. The explanation is based on the following flow.



① I/O board power supply

- The I/O board generates the reference voltage of the YTO and synthesizer. If the voltage is fault, no waveforms appear at the center of the screen even when the R3265/3271 is set to:

  CF 0MHz
  SPAN 1GHz

- Check the voltage at each test pin of I/O board shown in Figure 6-24.

Table 6-34 Voltages at Test Pin (I/O board)

Test Pin	Voltage
TP1	+14.5V
TP2	−12V
TP3	+10V
TP4	+5V

- If they do not match the voltages of Table 6-34, check the power supply of the I/O board.

② YTO TUNE

If the YTO tuning has failed, check the following:

(a) YTO TUNE DAC (U19, U20)

- Set the R3265/3271 to ZERO SPAN mode, and monitor the voltage at pin 6 of U20 with the following frequency:

Table 6-35 YTO TUNE DAC

Center Frequency	Voltage at pin 6 of U20
0 Hz	−0.88 V
3.6 GHz	−9.66 V

- If the voltage matches the one defined on Table 6-35, the YTO TUNE DAC is operating normally.

(b) 0 MHz ADJ and 3.5GHz ADJ boards

To check the 0 MHz ADJ and 3.5 GHz ADJ boards, set as follows:

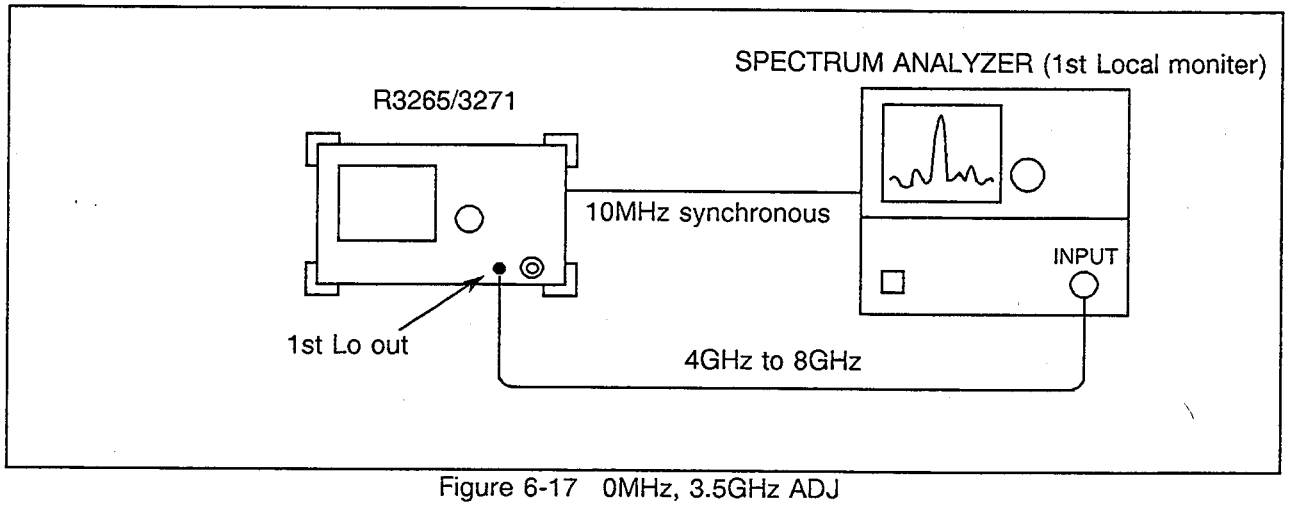
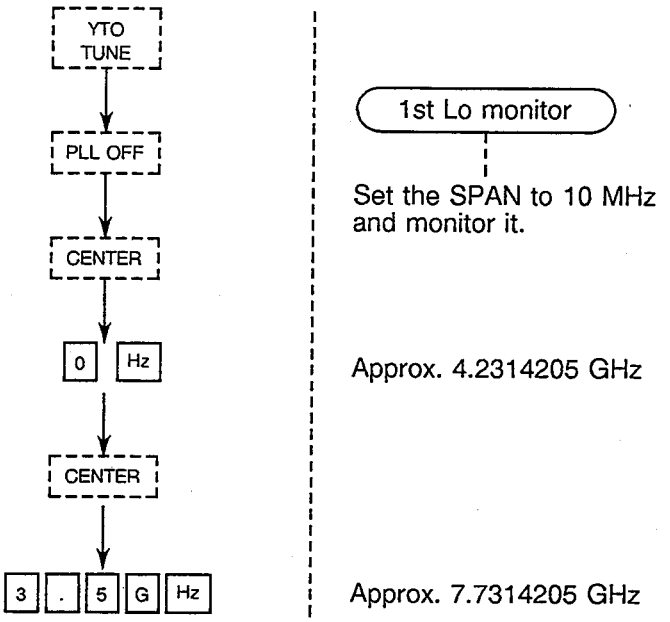


Figure 6-17 0MHz, 3.5GHz ADJ

Set the R3265/3271 to the ZERO SPAN to select the Maintenance mode, perform the following procedure, and monitor the 1st Local status during this time.



When this procedure is complete, the 0 MHz ADJ and 3.5 GHz ADJ boards have been adjusted.
If no waveforms appear on the monitor spectrum analyzer, check the following:

- If no waveforms appear during CF = 0 Hz

  Monitor the voltage at pin 7 of U22 of the I/O board on the DVM.
  Select the Maintenance mode, set CENTER 0 Hz and make sure that the voltage at pin 7 of U22 and the "1st Lo out" frequency change as follows when the data of 0 MHz ADJ is changed.

Table 6-36 0 MHz ADJ

Data of 0 MHz ADJ	Voltage at pin 7 of U22	"1st Lo out" frequency
00 (H) to ff (H)	0 V to −10 V	The frequency changes approx. 280 MHz via 4.2314205 GHz.

If the voltage is incorrect at pin 7 of U22, check the U21 and U22.
If the voltage is correct at pin 7 of U22 but if the "1st Lo out" frequency does not change approx. 280 MHz, check the U26 and Q11.

- If no waveforms appear during CF = 3.5GHz

  Monitor the voltage at pin 1 of U22 of the I/O board on the DVM.
  Select the Maintenance mode, set [CENTER] [3] [.] [5] [GHz] and make sure that the voltage at pin 1 of U22 and the "1st Lo out" frequency change as follows when the data of 3.5 GHz ADJ is changed.

Table 6-37 3.5 GHz ADJ

Data of 3.5 GHz ADJ	Voltage at pin 1 of U22	"1st Lo out" frequency
00 (H) to ff	0 V to −10 V	The frequency changes approx. 280 MHz via 7.7314205 GHz.

If the voltage is incorrect at pin 1 of U22, check the U21 and U22.
If the voltage is correct at pin 1 of U22 but if the "1st Lo out" frequency does not change approx. 280 MHz, check the U24 and Q10.
To release the Maintenance mode and return to the Normal mode, repeat pressing the [RETURN] software key.

③ Lamp voltage

Use the following procedure if the system is locked but the waveforms fail (Figure 6-18) (when the SINGLE sweep mode is selected and the "1st Lo out" is monitored).

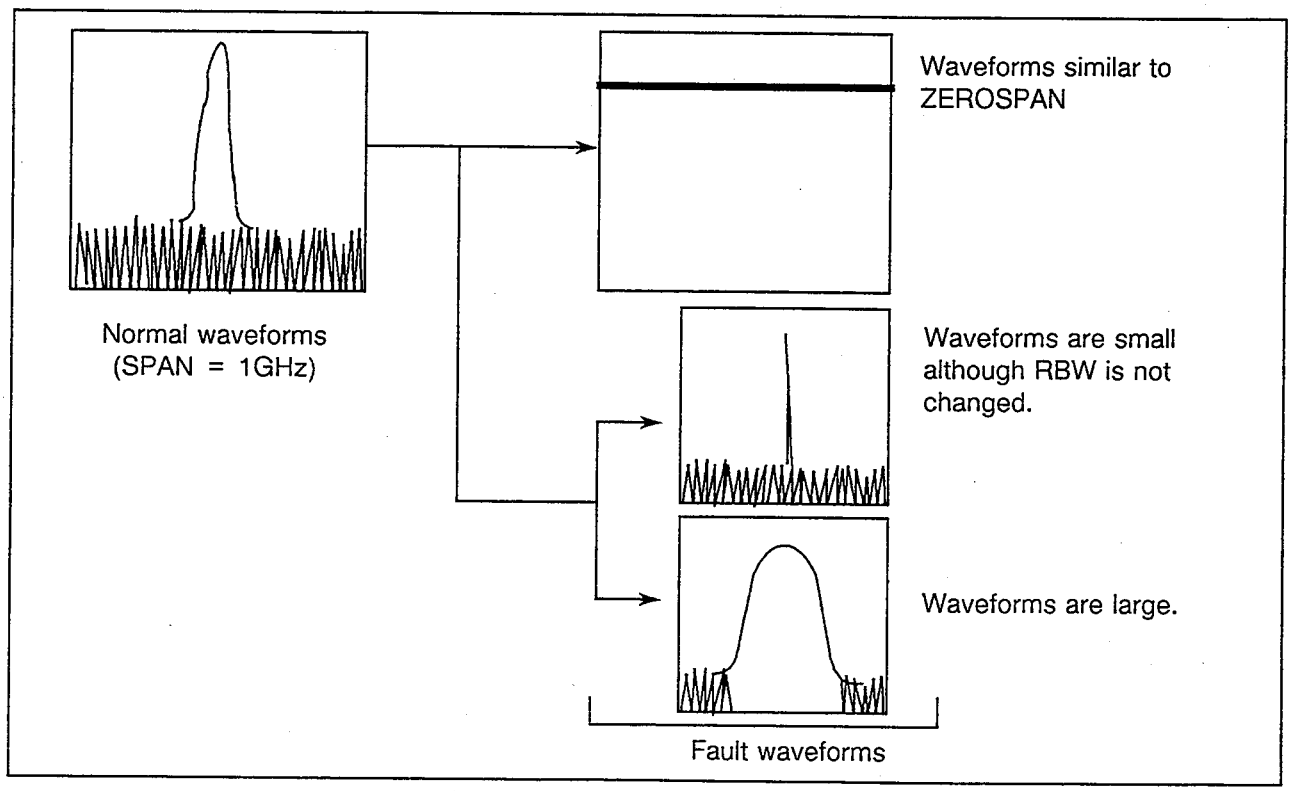


Figure 6-18 Fault Waveforms

Set the R3265/3271 as follows:

CF 0Hz
SPAN 1GHz
SWEEP MODE ..... CONT SWEEP

The lamp waveforms of each part are shown in Figure 6-19. However, the output voltage may have several percents of errors after the stage of pin 7 of U5 (SPAN ADJ OUT) due to the different YTO tuning sensitivity.

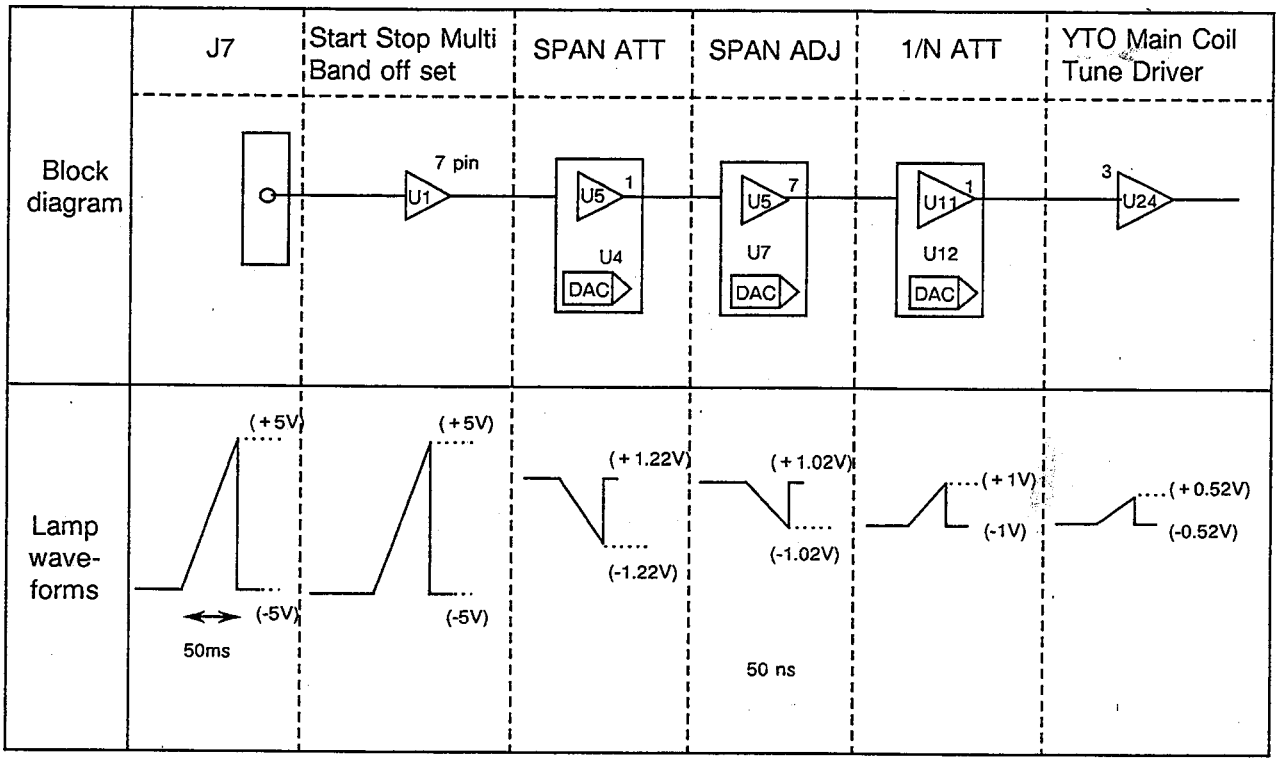


Figure 6-19 Lamp Waveforms of Each Part

(a) Start Stop Multiband Offset
If the output lamp voltage has failed at pin 7 of U1 although the normal lamp voltage appears at J7, the U1, U2 or U3 operation may have failed.

(b) SPAN ATT
If the output lamp voltage has failed at pin 1 of U5, the U5 or U4 may have failed.

(c) SPAN ADJ
If the output lamp voltage has failed at pin 7 of U5, check the U5, U6 and U7.

(d) 1/N ATT
If the output lamp voltage has failed at pin 1 of U11, check the U11 and U12.

(e) X10, X1, X0.1, and X0.01 ATT's

If the fault lamp voltage appears at pin 3 of U24 although the normal lamp voltage appear at 1/N ATT OUT, check the following points.

First, check the U16 and U17 control pin values.

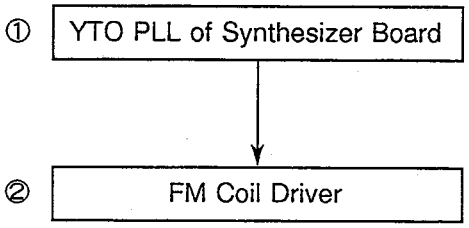
Table 6-38 X10, X1, X0.1, and X0.01 ATT's

Span	U16				U17			
	9pin	8pin	1pin	16pin	1pin	16pin	9pin	8pin
40 GHz > SPAN > 4 GHz	0	1	0	0	1	1	0	1
4 GHz ≧ SPAN > 400 MHz	1	0	0	1	1	1	0	1
400 MHz ≧ SPAN > 40 MHz	1	0	1	1	0	1	0	1
40 MHz ≧ SPAN > 10 MHz	1	0	1	1	1	0	0	1
10 MHz ≧ SPAN > 2 MHz	0	1	0	1	1	1	0	1
2 MHz ≧ SPAN > 400 kHz	0	1	0	1	1	1	1	0
400 kHz ≧ SPAN > 50 kHz	0	1	1	1	0	1	1	0
50 kHz ≧ SPAN > 2 kHz	0	1	0	1	1	1	1	0
2 kHz ≧ SPAN > ZERO	0	1	1	1	0	1	1	0
ZERO	0	1	1	0	1	1	0	1

If the signals defined on Table 6-38 appear at the control pins and if the fault lamp voltage appears at pin 3 of U24, the U16 operation may have failed.

(2) Problem in 500 MHz ≧ SPAN > 10 MHz

It is assumed that the YTO ADJ (0 MHz, 3.6 GHz) has been used, the Sampler PLL and VHF PLL have been locked, but the YTO PLL are unlocked. The explanation is based on the following control flow.



① YTO PLL of Synthesizer Board

Change the YTO frequency in the Maintenance mode and make sure that the Phase Detector of the YTO PLL operates normally. For details, see the "Unlocked YTO PLL" section.

② FM Coil Driver

After the YTO PLL of the synthesizer board has been checked, check the FM Coil Driver in the following procedure.
Unplug the connector from J8 of the I/O board, and plug the DC standard connector into it. Set the R3265/3271 as follows:

CF 0MHz
SPAN 20MHz
SWEEP MODE ..... SINGLE

Monitor the YTO oscillation frequency from the "1st Lo out" of the front panel.
Set the DC standard output voltage to +13V or −13V, and make sure that the voltage and frequency of each part match the ones defined on Table 6-39.

Table 6-39 FM Coil Driver

DC Standard	U30 6 pin	U18 14 pin	U28 6 pin	YTO frequency of 1st LO OUT
+13 V	+9.95V	+9.8V	−9.8V	Approx. 4.26GHz
−13 V	−9.9 V	−9.8 V	+9.8V	Approx. 4.2GHz

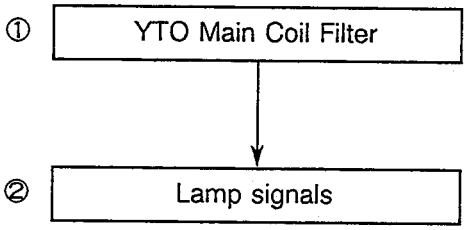
Also, make sure that the following signals appear at the U18 control pins.

Pin 1 ..... High
Pin 8 ..... High
Pin 16 ..... Low
Pin 9 ..... Low

If the voltage differs from the definition, troubleshoot its section. If the voltage is the same but the frequency differs, the U29, Q12 or YTO operation may have failed.
The signal path of the lamp voltage is the same as that described in the "Problems not associated with the span" section.
See the operation principle of I/O board although the various D/A set values are different.

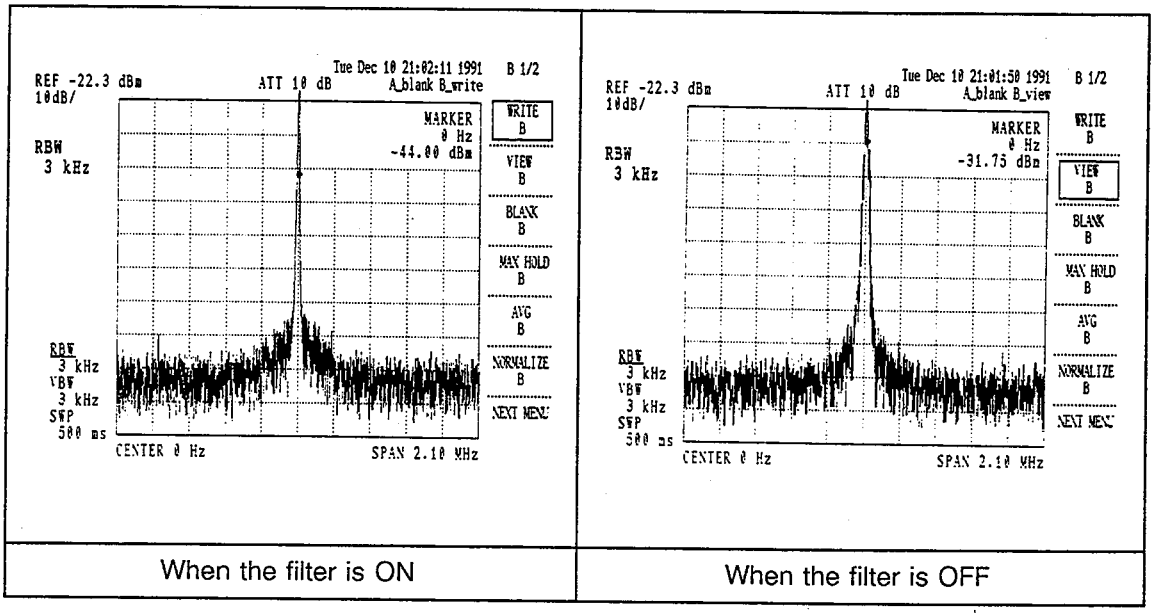
(3) Problems in 10 MHz ≧ SPAN > 2 MHz

In this span, the signal path during YTO PLL lock is the same as for 500 MHz ≧ SPAN > 10 MHz, except that the filter (R75, C31) is inserted in the Main Tune section and that the signal is swept using the FM Coil.
The explanation is based on the following control flow:



① YTO Main Coil Filter

The following compares the waveforms when the signals are passed through the YTO Main Coil Filter and when they are not passed.



When the filter is ON	When the filter is OFF

If the waveforms appear as if the filter is OFF, troubleshoot in the following procedure:

- Make sure that approx. +5V is entered in pin 2 of R72 and that approx. 0.7V appear at pin 2 of Q7.
- If they are correct and if the waveforms are distorted, the K1 may have failed.

If the waveform response is delayed when the SPAN mode is changed from "SPAN > 10 MHz" to "10 MHz ≧SPAM > 2 MHz", make sure that the voltage at pin 2 of R66 is roughly equal to the voltage at pin 1 of R75. If not, check the U23, Q8, and Q9.

② Lamp signals

Set the R3265/3271 as follows:

CF 0MHz
SPAN 10MHz
SWEEP MODE ..... CONT

Also, make sure that the U18 control pins have been set as follows:

Table 6-40 Voltage Setup at U18 Control Pins

Pin No. of U18	Voltage
1 pin	5V
8 pin	0V
9 pin	5V
16 pin	0V

Make sure that the lamp voltages are as follows:

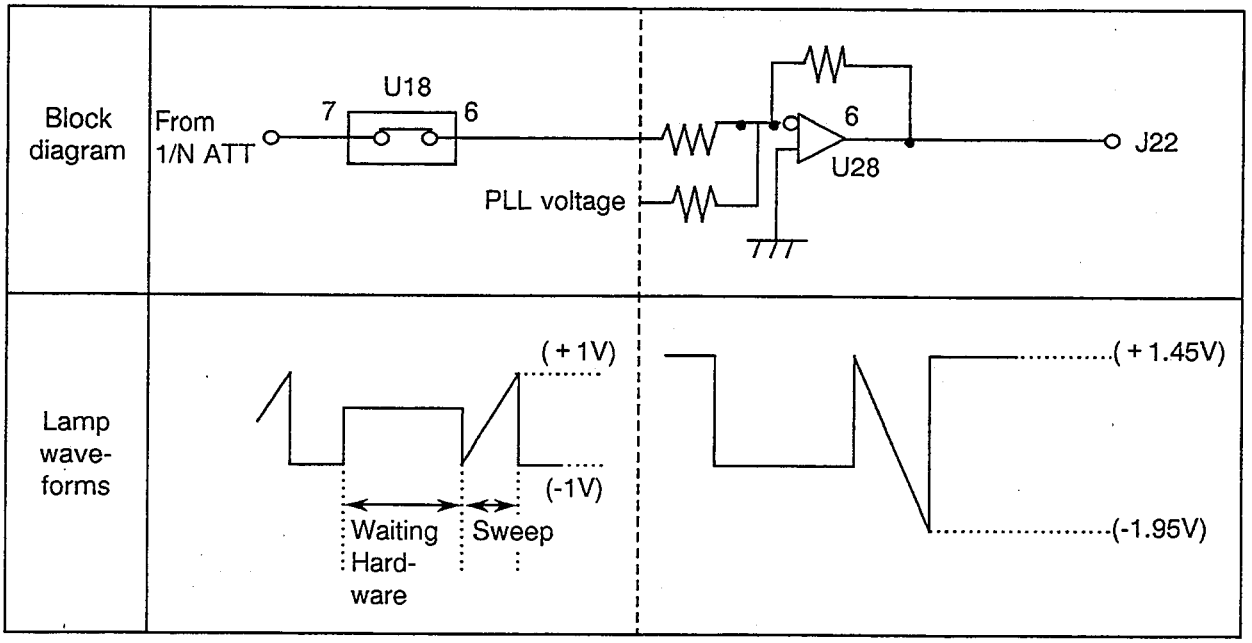


Figure 6-20 Lamp Waveforms of U18 and U28

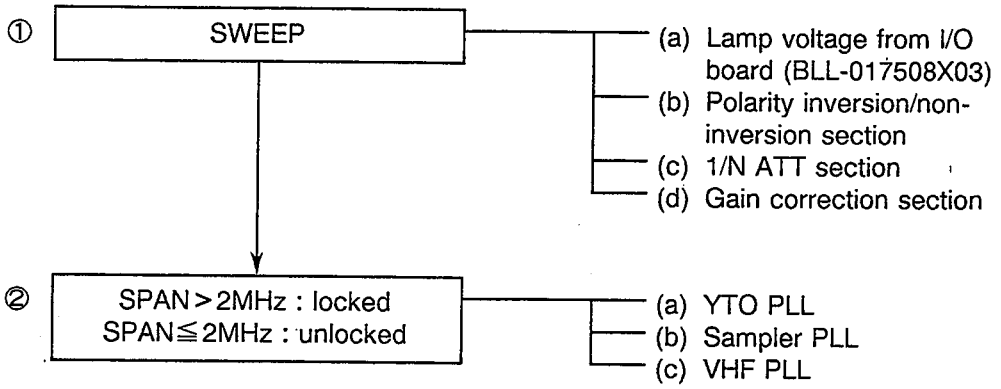
The lamp voltage at pin 6 of U28 are not at the 0V center position because the PLL voltage has been offset.

If the lamp voltage does not match Figure 6-20, check the U18 and U28.

If the lamp voltage has failed at pin 7 of U18, perform troubleshooting by referring to Item ③ of the "Problems not associated with the span" section.

(4) Problems if SPAN is less than 2 MHz

The following explains various problems in the sweep span of R1 PLL (2 MHz ≧ SPAN > 50 kHz) and sweep span of R2 PLL (50 kHz ≧ SPAN > 200 Hz).



The following explains the sweep failure below 2 MHz and lock failure. If the sweep fails if SPAN > 2 MHz, see the "Problems if SPAN>10 MHz" section or "Problems if 10 MHz ≧ SPAN > 2 MHz" section.
If the lock fails if SPAN > 2 MHz, see the "Unlock PLL" section.
Also, if the failure is detected in the Digital IF mode, see the "Unlocked PLL" section or refer to the Maintenance Manual of the IF board (BLS-017025).

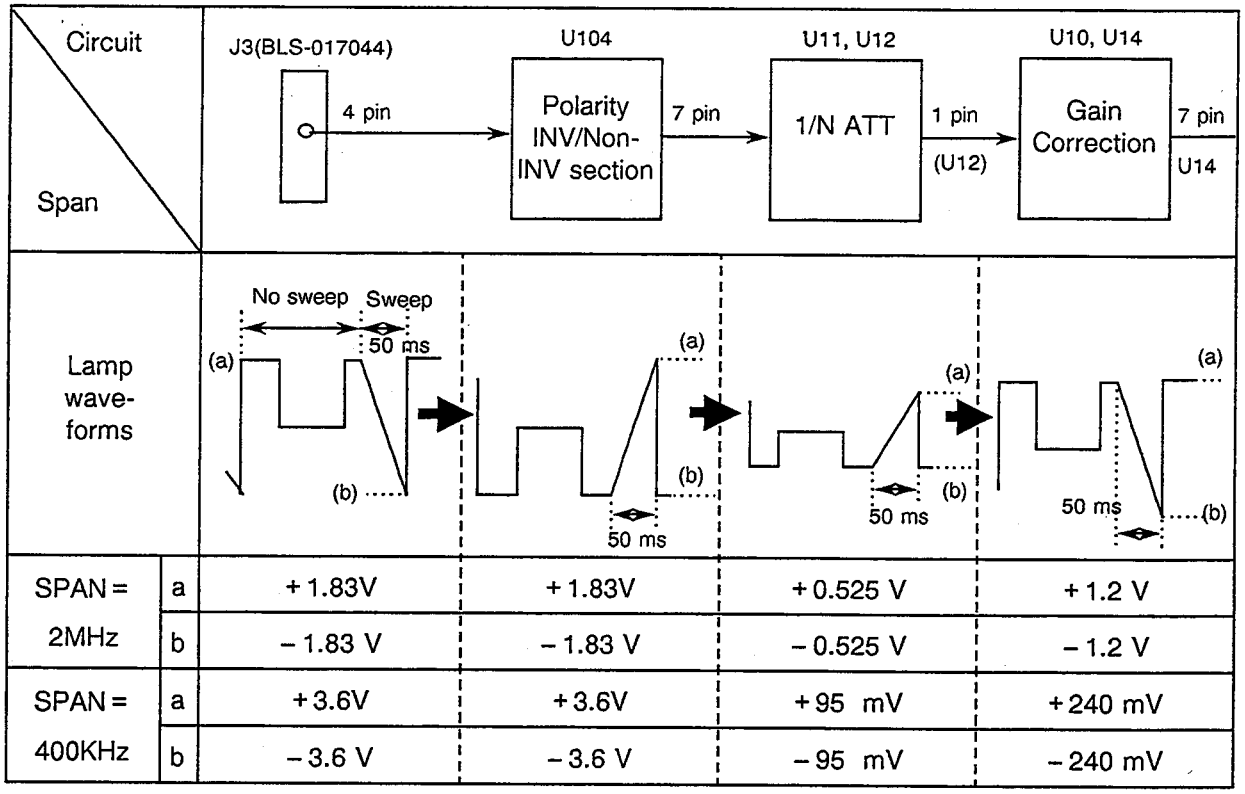
① SWEEP

If the desired frequency is locked (if the signal sweep is stopped in the SINGLE sweep mode, check its lock) and if the signal sweep fails for SPAN ≦ 2 MHz although the sweep for SPAN ≧ 2.01 MHz is normal, check the following points.
Set the R3265/3271 as follows:

CF 0MHz
SWEEP MODE ..... CONT SWEEP

The span is shown in Table 6-41. In other cases, it must be set to "AUTO". The voltages of Table 6-41 may differ from each other for the R3265/3271. They vary according to the difference of this system. The voltage at pin 7 of U14 may differ.

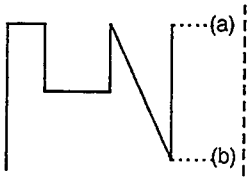
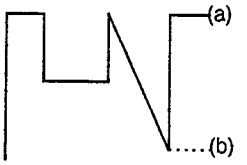
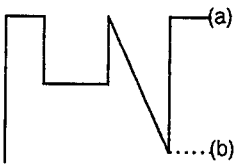
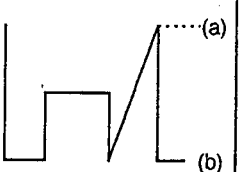
Table 6-41 Waveforms and Voltages if SPAN ≦ 2 MHz



SPAN = 2MHz	a	+1.83V	+1.83V	+0.525 V	+1.2 V
	b	−1.83 V	−1.83 V	−0.525 V	−1.2 V
SPAN = 400KHz	a	+3.6V	+3.6V	+95 mV	+240 mV
	b	−3.6 V	−3.6 V	−95 mV	−240 mV

The following shows the waveforms and voltages if SPAN ≦ 50 kHz.

Table 6-42 Waveforms and Voltages if SPAN ≦ 50 kHz

Circuit / Span		J3(BLS-017044) 4 pin	U104 Polarity INV/Non-INV section	U11, U12 1/N ATT	U10, U14 Gain Correction
Lamp waveforms					
SPAN = 50KHz	a	+ 1.8V	+ 1.8V	+ 0.52 V	+ 0.8 V
	b	– 1.8 V	– 1.8 V	– 0.52 V	– 0.8 V
SPAN = 20KHz	a	+ 1.8V	+ 1.8V	+ 0.52 V	+ 0.8 V
	b	– 1.8 V	– 1.8 V	– 0.52 V	– 0.8 V
SPAN = 2KHz	a	+ 1.8V	+ 1.8V	+ 48 mV	+ 78 mV
	b	– 1.8 V	– 1.8 V	– 48 mV	– 78 mV

If the 1/1 divider is used in the YTO PLL loop (that is, bit 7 of address 440160 is high), the voltage (p-p) at pin 4 of J3 is doubled. However, if 400 kHz ≧ SPAN > 50 kHz, the voltage at pin 4 of J3 remains unchanged. The voltage (p-p) of 1/N ATT OUT (at pin 1 of U12) is doubled.

(a) If the lamp voltage has failed at pin 4 of J3

- Check the cable continuity and shortcircuit of the cable between J9 of I/O board (BLL-017508X03) and synthesizer board (BLS-017044).
- If the cable is normal, troubleshoot the I/O board (BLL-017508X03).

(b) If the voltage has failed at the POLARITY INV/Non-INV section

- Check the U104 and U151 operations.

Pin 16 of U151	Polarity
High	Not inverted
Low	Inverted

(c) If the output voltage has failed at 1/N ATT section

- Check the U11, U151, and U12 operations.
  For the control signals of each span, see the 1/N ATT section of the lamp voltage of "each PLL control".

(d) If the output voltage has failed at the Gain Correction section

The voltage of this section may slightly vary according to the R1VCO and R2VCO characteristics. Perform the following procedure to check the U10 and U14 operations.
Set the R3265/3271 as follows:

CF 0MHz
SPAN 2MHz
SWEEP MODE . . . . . MANUAL

Move the marker to the leftmost end of the screen using the step key. Select the Debug mode, and write data "ff80" in address 440350.
If the voltage at pin 7 of U14 is 2 times larger than the voltage at pin 1 of U12, the Gain Correction section is normal during R1VCO sweep span (2 MHz ≧ SPAN > 50 kHz).
Then, set the R3265/3271 as follows:

CF 0MHz
SPAN 2MHz
SWEEP MODE . . . . . MANUAL

Move the marker to the leftmost end of the screen using the step key. Then, select the Debug mode and write data "ff80" in address 440340.
If the voltage at pin 1 of U14 is 2 times larger than the voltage at pin 7 of U12, the Gain Correction section is normal during R2VCO sweep span (50 kHz ≧ SPAN > 200 Hz).
If the span accuracy failure still exists, check the R1VCO and R2VCO. Also, check the pretune and linealizer sections.

② If the PLL is locked during SPAN ≧ 2.01 MHz but unlocked during SPAN ≦ 2 MHz

The PLL setup difference must be found for SPAN > 2 MHz and for SPAN ≦ 2 MHz. See the "each PLL control" section.

(a) YTO PLL

The YTO PLL has the loop filter whose span changes as shown on Table 6-43.

Table 6-43 YTO PLL Loop Filter

Span	Loop Filter
SPAN > 2 MHz	MID
2 MHz≧SPAN>200 kHz	NARROW
200 kHz≧SPAN	WIDE

It is very few that the PLL is locked during SPAN > 2 MHz due to YTO PLL failure but it is unlocked during SPAN = 2 MHz.
If the PLL is normal during SPAN > 200 kHz but if waveforms on the screen are deformed (as if the noise exists) during SPAN ≦ 200 kHz, check the following:

- Make sure that the FM Coil Driver (U30, U28, U29, Q12, and Q3) of the I/O board (BLL-017508X03) is not oscillating.
- Check whether the YTO PLL filter is switched according to the specific span or not.

(b) Sampler PLL

For the Sampler PLL, the loop filter changes in the span shown on Table 6-44.

Table 6-44 Loop Filter of Sampler PLL

Span	Loop Filter
SPAN > 2 MHz	WIDE
160 kHz<SPAN≦2 MHz	MID
SPAN≦160 kHz	WIDE

If noise appear on the waveforms at the boundary of SPAN = 160 kHz

- Make sure that the filter of Sampler PLL is switched according to the specific span.
- Make sure that the Sampler VCO has been adjusted correctly.

(c) VHF PLL

There is no control line where the R2 PLL and Offset PLL vary during SPAN > 2 MHz or SPAN ≦ 2 MHz.
If the PLL is unlocked during 2 MHz ≧ SPAN > 50 Hz only, the pretune voltage of R1 PLL may have failed. Also, if the PLL is locked during SPAN > 2 kHz but it is unlocked during SPAN ≦ 2 kHz, check the Reference Frequency section (U152, U153, U31) of R2 PLL.

6.8.3 Unlocked PLL

This section explains the troubleshooting to be used if each oscillator operates at the frequency different from the set value although no signal is swept (zero span in SINGLE sweep mode). Use a spectrum analyzer (covering up to 8 GHz, if any) and the probe. (The R3265/3271 must be synchronized with the 10 MHz signals). This explanation refers to Figure 6-22.
The following lists the measuring points of each PLL oscillation frequency.

YTO PLL ..... 1st LO OUT of the front panel
Sampler PLL ..... P2 of Sampler Synthesizer Block of Figure 6-22
R1 PLL ..... R1 TST of R1 Synthesizer Block of Figure 6-22
R2 PLL ..... R2 TST of R2 Synthesizer Block of Figure 6-22
Offset PLL ..... P12 of Offset Synthesizer Block of Figure 6-22

Measure signals at J2 to J8 of synthesizer board of Figure 6-24 for the Reference PLL. As the signal cables are been connected to these connectors, they must be unplugged before measurement. Table 6-45 provides the affects on the set frequency and signal level of each connector when it is unplugged.

Table 6-45 Each Connector of Reference PLL

J No. of Synt. Board of Fig. 6-24	Set Frequency	Signal Level	Results when unplugged
J2	200 MHz	+2 dBm	The 2nd PLL is unlocked.
J3	400 MHz	+3 dBm	
J4	400 MHz	+3 dBm	3rd PLL is unlocked.
J5	25 MHz	+1 dBm	Waveforms disappear during RBW ≦ 100 kHz.
J6	25 MHz	−10 dBm to −30 dBm	The output disappears at CAL OUT of front panel.
J7	80 MHz	+1 dBm	The CPU does not operate.
J8			The Reference PLL is unlocked.

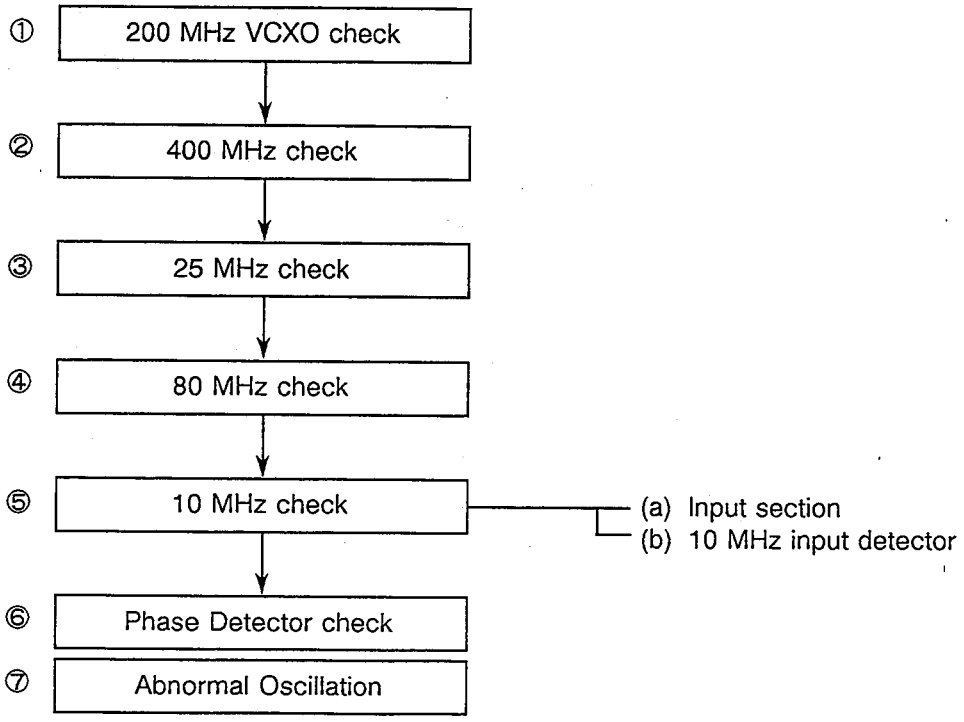
No cable is connected to J3. (If the cable connected to J4 is plugged into J3, no operational problem occurs.)
The 10 MHz signals are entered in J8 from the 10MSTD (BLB-017041) board.
The above listed measurement must be performed when all PLL's are locked (after the signal has been swept in the SINGLE sweep mode). If the measured frequency differs from the set frequency (see the "Maintenance mode" section), troubleshoot this PLL.

CAUTION

- It is assumed that the set frequency of each PLL and the M-time set value of Sampler PLL are known during PLL troubleshooting. For details, see the "Maintenance mode" section.
- It is assumed that the PLL has been locked during troubleshooting of this section. Select the SINGLE sweep mode unless otherwise noted.
- Start troubleshooting only after the correct YTO adjustment has been checked. (For details, see the YTO TUNE item of "Problems not associated with the span" section.)

(1) Unlock Reference PLL

The Reference PLL receives 10 MHz signals from the 10MSTD and locks the 200 MHz VCXO. The 200 MHz signals are used by the 2nd PLL. This 200 MHz signals are doubled and the resultant 400 MHz signals are used by the 3rd PLL, Sampler PLL, and VHF PLL.
The 25 MHz signals are generated from 400 MHz signals divided by 1/16. They are sent to the IF board (BLS-017025), CAL OUT and others. The 80 MHz signals are generated from 400 MHz signals divided by 1/5. They are sent to the CPU board (BLS-017500).
As the Reference PLL is associated with a large number of boards and blocks, the unlocked PLL affects on many points.
The description is based on the following control flow (see Figure 6-22).



① 200MHz VCXO Check

The signal having approx. 200 MHz frequency at +2 dBm level is output at pin 2 of 200 MHz VCXO. If the signal having approx. 200 MHz frequency at +10 dBm level or more is not output at pin 1 of L7, check the Q1 and Q3.

② 400MHz Check

The signal having approx. 400 MHz frequency at approx. 0 dBm level is output at pin 1 of FL1. If not, check the L7, L8, D1, and D2.

If the normal signals is output at pin 1 of FL1 but if the signal having approx. 400 MHz frequency at −5 dBm level is not output at pins 4, 5, 6, and 9, check the Q10, Q9, Q8, Q6, and Q5.

③ 25MHz Check

If the 25 MHz output signal level (at J5 of Figure 6-24) is −2 dBm or less although the Reference PLL is locked, check the U8, U9, and U10.

The 400 MHz input signal level into U8 is approx. 0 dBm.

④ 80MHz Check

If the 80 MHz output signal level (at J7 of Figure 6-24) is −2 dBm or less although the Reference PLL is locked, check the U3 and U4. The 400 MHz input signal level of U3 is approx. +4 dBm.

If the voltage at pin 14 of U3 is not equal to approx. 3.5V, the U3 may have failed.

⑤ 10MHz Check

(a) Input section

If the TTL level signal is not output at pin 1 of U14 although the signal having the 10 MHz frequency at −2 dBm level is output at pin 18, check the U13, FL5, Q15, and Q16.

If the signal at −2 dBm level or more is not output at pin 18, check the continuity and shortcircuit of the cable connected from the 120MHz STD or 10MHz STD.

(b) 10 MHz input detector

If the TTL level signal having the 10 MHz frequency is not output at pin 11 of U15 although it is output at pin 1 of U14, check the U14, D3, C93, and U15.

⑥ Phase Detector Check

Send an output of Signal Generator to J8 of Figure 6-24.
Set the Signal Generator as follows:

CW 10MHz
LEVEL ..... +0dBm

If the TTL level signals having 10 MHz frequency are not output at pin 1 of U16, check the U3, U5, and U6.
When the normal signals appear at pin 1 of U16, change the frequency of Signal Generator and make sure that the voltage at pin 1 of 200 MHz VCXO changes as shown on Table 6-46.

Table 6-46 Voltage at Pin 1 of 200 MHz VCXO

SG Frequency	Voltage at Pin 1 of 200 MHz VCXO
10.1 MHz	+13 V
9.9 MHz	−13 V

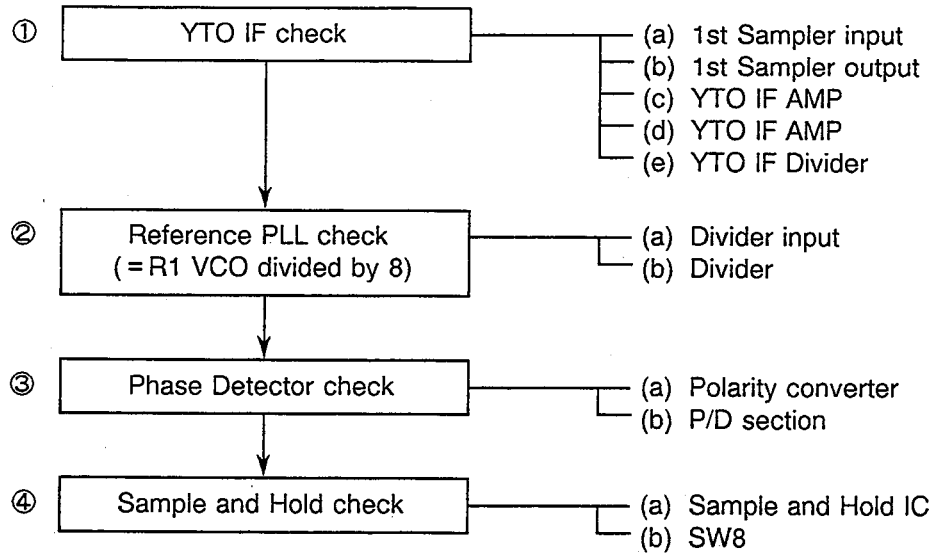
If the voltage is not switched, check the U16, U15, and Q17 to Q20.

⑦ Abnormal Oscillation

If the 200 MHz VCXO still oscillates abnormally or if its oscillation is stopped, replace the 200 MHz VCXO.

(2) Unlocked YTO PLL

Use the troubleshooting procedure of this section if the measured oscillation frequencies of Reference PLL, Sampler PLL, and VHF PLL are the same as their set values (during Zero Span or SINGLE sweep mode), but the measured oscillation frequency of YTO PLL differs from its set value.
If a PLL other than YTO PLL is unlocked, troubleshoot it first.
The YTO PLL receives the M-time RF signals of Sampler PLL oscillation frequency and the YTO oscillation frequency, generates the YTO IF signals, and locks the PLL using this YTO IF and R1 VCO oscillation frequencies. See the Synthesizer Block of Figure 6-22.
The explanation of this section is based on the following control flow.



① YTO IF signal level check

CAUTION

The YTO adjustment means the selection of Maintenance mode and adjustment of YTO TUNE. Do not write the adjusting value in the ROM during troubleshooting. For details, see the "YTO TUNE" paragraph of "Problems not associated with span" section.

(a) 1st Sampler (THD-295) input

- Make sure that the YTO signal of approx. −10 dBm level is sent from the 1st ISO AMP to the 1st Sampler.
- If it is not approx. −10 dBm, check the 1st ISO AMP or check the cable conductivity or shortcircuit.

(b) 1st Sampler (THD-295) output

- Connect a spectrum analyzer to the "1st LO OUT" terminal of the front panel, and monitor the YTO oscillation frequency.
- Select the Maintenance mode, press the [YTO TUNE] and [PLL OFF] keys, and adjust the set value of YTO oscillation frequency within ±2 MHz by observing the spectrum analyzer connected to the "1st LO OUT".

- On the spectrum analyzer, make sure that the signals having the frequency similar to the YTO IF set value (within ± several MHz) at approx. −30 dBm level are output at pin 22.

- If approx. −30 dBm signals are not output, the 1st Sampler may have failed.

(c) YTO IF AMP

- Set the YTO in the same conditions as Step (b) and perform troubleshooting.

- Make sure that the signals having the frequency (within ± several MHz) similar to the YTO IF at the ECL level appears at pin 6 of U86.

- If the normal voltage is not entered, measure the voltage at pin 3 of U168. It must be approx. +5V.

(d) YTO IF AMP

If the signal is not approx. +5V, check the Q105. If it is approx. +5V but the normal signal is not entered in pin 6 of U86, the YTO IF AMP of U168, U83, or U84 may have failed.

(e) YTO IF Divider

- Set the YTO in the same conditions as Step (b) and perform troubleshooting.

Table 6-47 Signal Frequency at Pin 2 of U165

Pin 13 of U165	Signal Frequency at Pin 2 of U165
High	Same as YTO IF
Low	Same as YTO IF divided by 2

- Make sure that the U165 functions as defined on Table 6-47. If not, check the U86 and U165.

② Reference PLL check (=R1 VCO divided by 8)

(a) Divider input

- Make sure that the signal having the R1 PLL set frequency at −10 dBm or more level appears at pin 11.

- If the signal level is too low or no signal appears, monitor the signal at pin 13 of R1 Synthesizer block. If the fault recurs, check the R1 PLL. If incorrect, check the shielded jumpers connected from pin 13 to pin 11 for their shortcircuit or open.

(b) Divider

- Make sure that the ECL level signal having the R1 PLL set frequency divided by 8 is output at pin 2 of U88. If not, check the divider of U87 and U88.

③ Phase Detector check

Set the R3265/3271 and monitor SPA in the same status as that used in substep (b) of Step ①.

(a) Polarity converter
Assume that signal A (R1/8) is entered in pin 5 of U79 and that signal B (YTO IF divided by 2 or YTO IF) is entered in pin 12 of U79.

Table 6-48 Signals of Polarity Converter

Pin 4 of U79	Pin No. of signal A output	Pin No. of signal B output
High	Pin 14 of U79	Pin 3 of U79
Low	Pin 3 of U79	Pin 14 of U79

(b) Phase Detector section
Make sure that the P/D section operates normally during YTO adjustment.

Table 6-49 Voltage at Pin 1 of U81

	YTO set frequency > YTO	YTO set frequency < YTO
Voltage at pin 1 of U81	Approx. +12V	Approx. −12V

If the result is abnormal, check the Phase Detector (U80, U81).

④ Sample and Hold section

(a) Sample and Hold IC
Set the R3265/3271 as follows:

CF 0MHz
SPAN 2.01MHz
SWEEP MODE ..... MANUAL SWP

Observe the voltage appearing at pin 5 of U82 on the DVM and rotate the encoder control of the R3265/3271. If the voltage changes very few, the Sample and Hold section operates normally.
This rule also applies to the voltage at pin 17.

(b) SW8 (Figure 6-22)

Set the R3265/3271 as follows:

CF 0MHz
SPAN 2MHz
SWEEP MODE ..... SINGLE SWP

Set the R3265/3271 and the monitor SPAN to the same status that was used in substep (b) of Step ①.

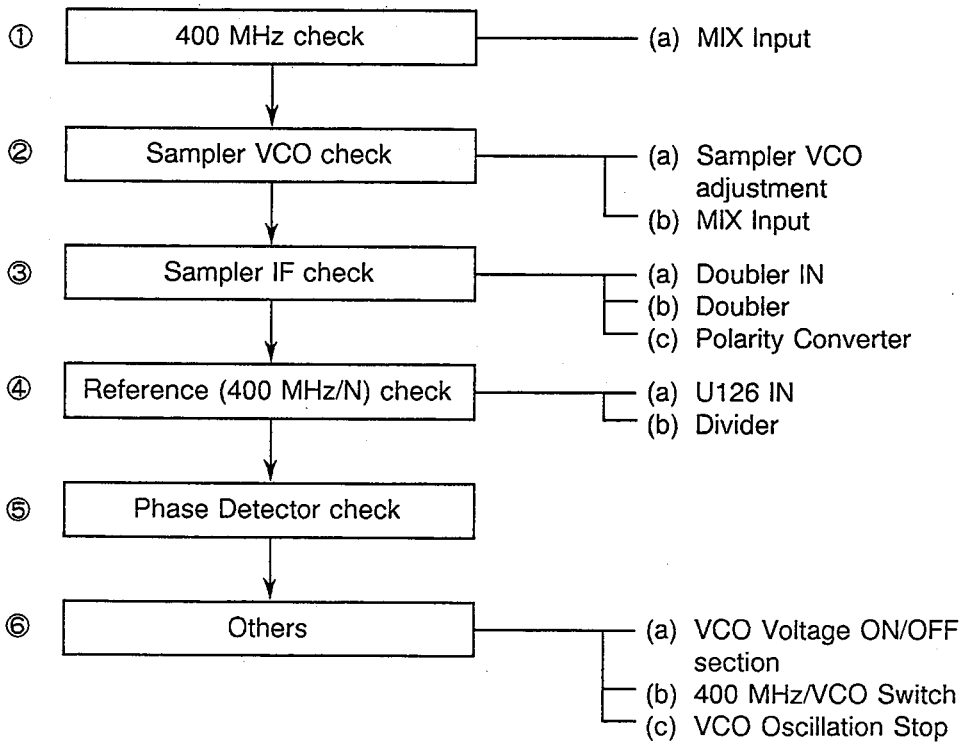
Adjust the YTO to change the +12 or −12V voltage at pin 1 of U81. (For YTO adjustment, see the YTO TUNE item of the "Problems not associated with the span" section.) The voltage at pin 17 also changes according to the voltage at pin 1 of U81. If not, the U161 may have failed.

(3) Unlocked Sampler PLL

If the measured value of the Reference PLL is same as its set value but if the measured value of oscillation frequency differs from its set value, perform the following troubleshooting procedure.

The Sampler PLL receives 400 MHz signals from the Reference PLL and the oscillation frequency signals from the Sampler VCO, and generates Sampler IF signals. This Sampler IF signals and the divided 400 MHz signals sent from the Reference PLL are used for PLL lock. The Sampler PLL may output the Sampler VCO signals or 400 MHz signals.

The following explanation refers to Figure 6-22, and it is based on the following control flow.



① 400 MHz check

(a) MIX Input

The 400 MHz frequency signals at approx. +8 dBm level must appear at pin 2 of MIX4. If the signal level is low, measure the 400 MHz signal frequency at pin 1. It must be approx. 0 dBm at pin 1. If it is low, check the shielded jumpers for shortcircuit or open between pin 6 of Reference PLL and pin 8 of Sampler PLL.
If the signal level at pin 1 is normal, check the 400 MHz ISO AMP of Q76, Q77 and Q78.

② Sampler VCO check

(a) Sampler VCO adjustment

Set the R3265/3271 as follows:

CENTER 40MHz
SPAN 10MHz

Monitor the signal at pin 2 on the spectrum analyzer. The analyzer must be set as follows:

CENTER 400MHz
SPAN 10MHz

Shortcircuit the J5 line of the Sampler synthesizer block and adjust R589 to have the 400 MHz waveforms on the monitor screen.
If this adjustment has failed, check the voltage at pin 1 of Sampler VCO. To do so, keep the J5 shortcircuited and fully rotate the control (R589) counterclockwise and then clockwise and make sure that the voltage changes between approx. −11V and −4V at pin 5 of Sampler VCO. If not, check the U125 and U121.
If the control functions normally and if the Sampler VCO cannot be adjusted to 400 MHz, replace the Sampler VCO.
After the Sampler VCO has been replaced due to a problem, this 400 MHz adjustment is always required. Open the shortcircuited J5 line at the end of adjustment.

(b) MIX Input

If the output signal level is approx. 0 dBm at pin 3 of Sampler VCO (U119) and if the signal having the same frequency with −15 dBm level appears at pin 4 of MIX, check the Q71, Q73, Q74 and Q75.

③ Sampler IF check

(a) Doubler IN

If the signal at pin 5 of L102 is −5 dBm or less, the MIX4 or U128 may have failed.

(b) Doubler

If the signal frequency at pin 4 of U122 is not equal to a double of the frequency at pin 6 of L102 during Doubler ON (see the Sampler PLL section of each PLL control), check the L102, D45, D46, and U121.

(c) Polarity Converter

Convert the bit-0 data at address 440120 (see the Sampler PLL section of each PLL control) from logical 1 to 0, and make sure that the signal logic changes from high to low at pin 2 of U134. Also, make sure that the same frequency signal appears at pins 9 and 6 of U135 and at pins 2 and 8 when the signal is low at pin 2 of U134. Also, make sure that the same frequency signal appears at pins 9 and 8 of U135 and at pins 2 and 6 when the signal is high at pin 2 of U134.

④ Reference (400 MHz/N) check

(a) U126 IN

Make sure that the 400 MHz frequency signals at +1 dBm level are entered at Pin 15 of U126. If not, the Q82 may have failed.

If approx. +3.5V do not appear at pin 14 of U126, the U126 may have failed.

(b) Divider

For the divider set data, see the "Maintenance mode" section.

If the data is not entered normally into the divider from the latch, the U6 may have failed or the data line may have been opened or jumpered.

If the data is entered normally but the signal with the 400 MHz frequency divided by "N" does not appear at pin 2 of U135, check the divider.

⑤ Phase Detector check

Remove the shielded jumper from pin 1 of the 400M IN, and enter signals of the Signal Generator.

Set the R3265/3271 as follows:

CF 0MHz
SPAN 2MHz
SWEEP MODE ..... SINGLE

Change the frequency of the Signal Generator with the 0 dBm fixed output level as defined on Table 6-50, and monitor the voltage at pin 5 of Sampler VCO.

Table 6-50 Voltage at Pin 5 of Sampler VCO

SG Frequency	Voltage at Pin 5 of Sampler VCO
420MHz	−6V
390MHz	−11V

If the voltage given on Table 6-50 is obtained, the Phase Detector operates normally.

⑥ Others

(a) VCO Voltage ON/OFF section

Convert the bit-1 data at address 440120 in the Debug mode and make sure that the voltage changes at pin 2 of Sample VCO.

Table 6-51 Voltage at Pin 2 of Sampler VCO

Data	Voltage at Pin 2
1	Approx. 0V
0	Approx. −14.2V

If the voltage given on Table 6-51 is obtained, the VCO Voltage ON/OFF section operates normally.
If not, check the Q79, Q80 and Q81.

(b) 400 MHz/VCO Switch

Set the bit-1 data at address 440120 as defined on Table 6-52 and monitor the voltage at pin 1 of U125.

Table 6-52 Voltage at Pin 1 of U125

Data	Voltage at Pin 1
1	−11.5V
0	+11.5V

If the signal frequency is not switched between the Sampler VCO and 400 MHz at pin 2 although the voltage is switched normally at pin 1 of U125, check the Q72, and D39 to D43.

(c) VCO Oscillation Stop

If the Sampler VCO has stopped in its oscillation, check the following points:

- Approx. −14.2V must appear at pin 2 of Sampler VCO and approx. −13.5V must appear at pin 1.
- Each function must be normal at each signal level when the Sampler VCO is forcibly oscillated in the same status as that used in substep (a) of Step ②.
  If no fault is found, replace the Sampler VCO.

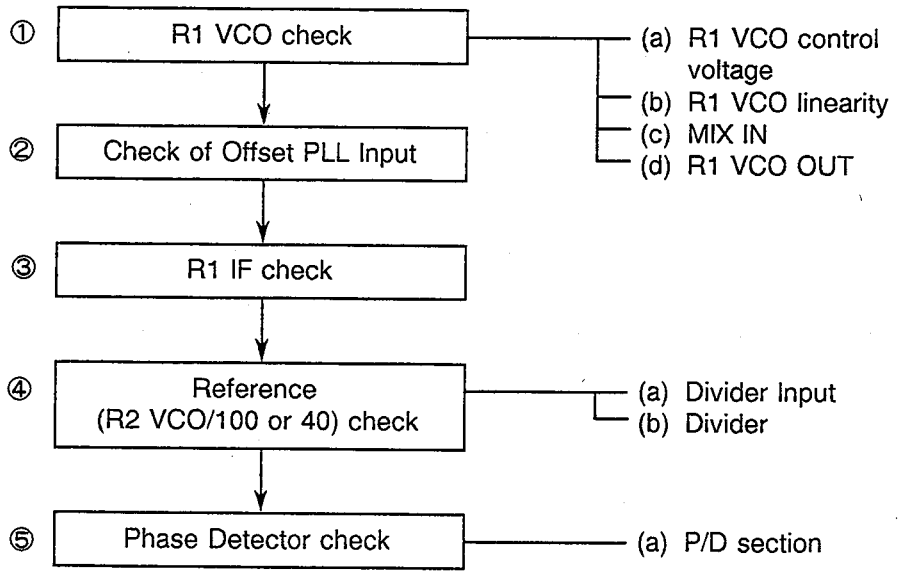
(4) Unlocked R1 PLL

If the measured oscillation frequencies of the Reference PLL, Offset PLL, and R2 PLL are the same as their set values but if the measured oscillation frequency of R1 PLL differs from its set value, perform the following troubleshooting procedure.

The R1 PLL receives the signal oscillation frequency of the Offset PLL and the R1 VCO signals, and generates R1 IF signals. The R1 IF and divided R2 VCO signals are used for PLL lock. The R1 PLL has the Sample and Hold IC, and it sweeps signals at the pretune voltage that is entered from pin 14 if 2 MHz ≧ SPAN > 50 kHz.

To check the unlocked PLL, select the SINGLE sweep mode. See the R1 block diagram of Figure 6-22.

The explanation is based on the following control flow:



① R1 VCO check

(a) R1 VCO control voltage

Make sure that the voltage is within +8.7 ±0.5V at pin 2 of R645 (at the opposite side of GND pin) locating close to pin 5 of R1 VCO. If not, check the voltage at each point of Q91.

(b) R1 VCO linearity

Set the R3265/3271 as follows:

CF 0Hz
SPAN 2MHz
SWEEP MODE ..... SINGLE

After a single sweep has completed, perform the following:

Remove the R229 from the board. It locates close to pin 5 of R1 VCO. Then, monitor the voltage at pin 5 of R1 VCO on the DVM and monitor the signal frequency at P32 using the spectrum analyzer.

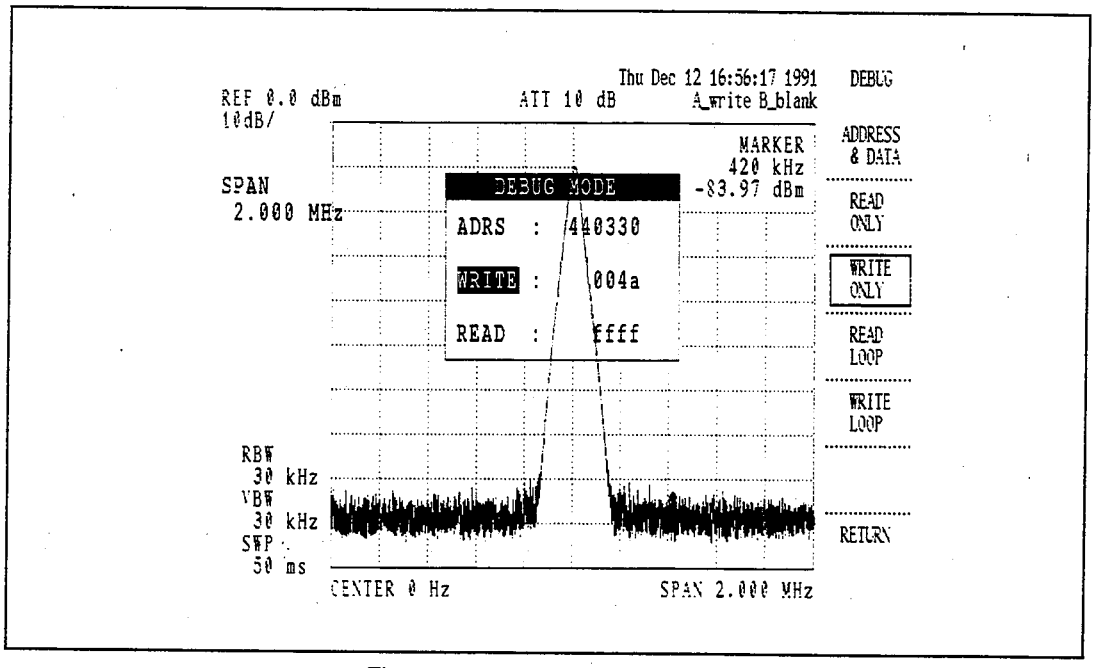


Figure 6-21 R1 VCO Check

Select the Debug mode, enter address 440330, and press the WRITE ONLY key (see Figure 6-21). Rotate the encoder control to change data between "0000" and "00ff". At this time, make sure that the monitor voltage and frequency reaches the ones defined on Table 6-53.

Table 6-53 Voltage at Pin 5 of R1 VCO

Data	Voltage	Frequency
0000 to 00ff	Approx. 7.5V to Approx. −10V	413 MHz to 420 MHz to 535 MHz to 542 MHz

Also, make sure that the signal frequency of P32 changes according to the encoder adjustment.
If the voltage is abnormal, see the "Pretune Linealizer" section. If the signal frequency is abnormal, the VCO may have failed.

(c) MIX IN

Rotate the encoder control in the same status as that used in substep (b) to have the 470 MHz output frequency at pin 4 of R1 VCO. At this time, make sure that the signal level is approx. 0 dBm at pin 4 of R1 VCO.
Also, make sure that the 470 MHz frequency signal at +4 dBm level is entered in pin 3 of MIX3.

(d) R1 VCO OUT (TO YTO PLL)
Monitor the P13 signal in the same status as substep (c). Make sure that the signal has the 470 MHz frequency at −10dBm or higher level.

② Check of Offset PLL Input

Make sure that the signal having the oscillation frequency of Offset PLL at −13 dBm or higher level is entered in pin 3 of MIX4.

③ R1 IF check

In the same status as substep (b) of Step ①, rotate the encoder control to have the 470 MHz oscillation frequency of the R1 VCO.
If the normal input is entered in pins 4 and 3 of MIX3, if the signal frequency at pin 13 of U64 is equal to the "frequency at pin 4 of MIX3" subtracted by the "frequency at pin 3 of MIX3", and if the signal is not the TTL level signal, check the MIX3, LPF, U68, and U69.

④ Reference (R2 VCO/100 or 40) check

(a) Divider Input
If the signal frequency at pin 2 of U63 is the same as the R2 VCO oscillation frequency but if the signal level is below −5 dBm, the U36 may have failed.

(b) Divider
If the normal input is not found at pin 2 of U63, check the signal at pin 8 of U167 whether it matches the definition of Table 6-54 or not. The signal is high at pins 7 and 6 of U63. Change the data in the Debug mode.

Table 6-54 Signal Frequency and Level at Pin 8 of U167

Input Data at Address 440000	Frequency at Pin 8 of U167	Signal level at Pin 8 of U167
0e	R2 VCO oscillation f/100	TTL
2e	R2 VCO oscillation f/40	TTL

If they differ from the definition of Table 6-54, check the U63, U70, U167, and U71.

⑤ Phase Detector check

In the same status as substep (b) of Step ①, rotate the encoder control to adjust the R1 VCO oscillation frequency to 470 MHz. At this time, make sure that the normal signals are entered into pins 1 and 13 of U64.
Monitor the signal at pin 3 of U66 on the DVM and make sure that its voltage matches the one defined on Table 6-55.

Table 6-55 Signal Voltage at Pin 3 of U66

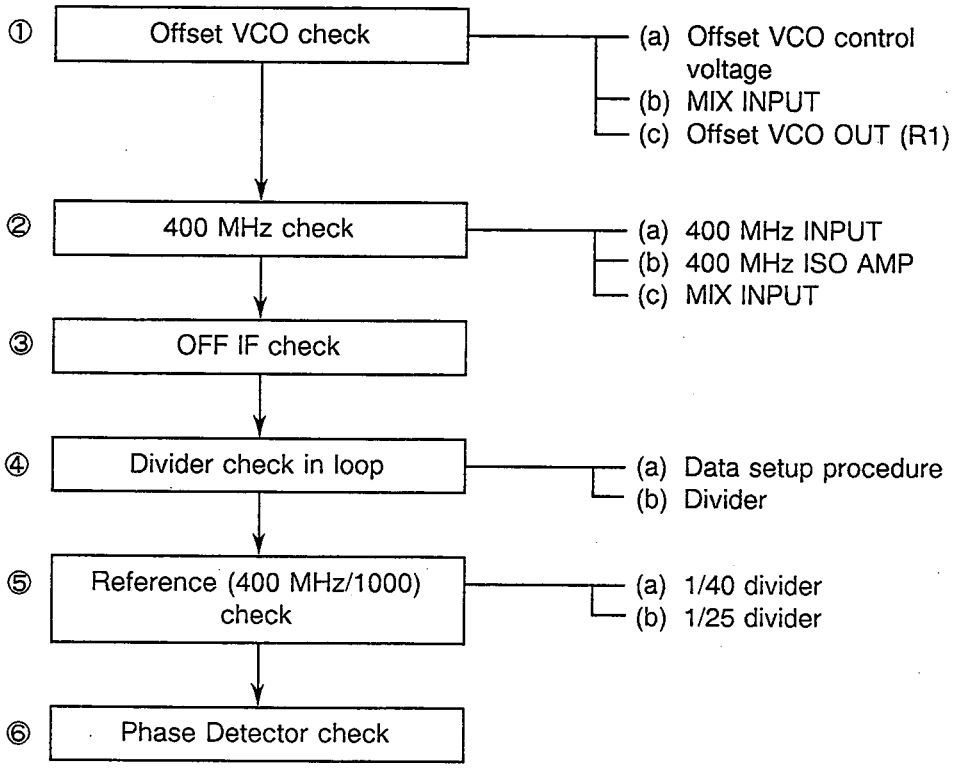
R1 VCO Oscillation Frequency (set by Encoder)	Voltage at Pin 3 of U66
471MHz	Approx. −12V
465MHz	Approx. +12V

(5) Unlocked Offset PLL

If the measured oscillation frequency of Reference PLL is the same as its set value but if the measured oscillation frequency of Offset PLL differs from its set value, perform the following troubleshooting procedure.

The Offset PLL receives 400 MHz signals sent from the Reference PLL and the oscillation frequency signals of Offset VCO, and generates OFF IF signals. These OFF IF signals and the 400 MHz signals divided by 1000 are used for PLL lock.

To check the unlocked PLL, select the SINGLE SWEEP mode. See the Offset PLL block diagram of Figure 6-22. The explanation is based on the following control flow.



CAUTION

If the signal level cannot be measured normally due to abnormal oscillation of Offset VCO or others, remove the R172 from the board. Then, connect the Signal Generator to the PAD connected to pin 2 of C136, and use it instead of the Offset VCO.

① Offset VCO check

(a) Offset VCO control voltage
Make sure that the voltage is approx. −12.2V at pin 1 of Offset VCO.

(b) MIX INPUT
If the signal level at pin 4 of Offset VCO is approx. 0 dBm and if the signal level at pin 3 of MIX2 is +4 dBm or less, check the Q24, U56, U57, and Q25.

(c) Offset VCO OUT (R1)
If the frequency level of the Offset VCO of P12 is −10 dBm or less, check the U55.

② 400 MHz check

(a) 400 MHz INPUT
If the 400 MHz signal level of P21 is −5 dBm or less, check whether the signal level of P9 is low or not at the Reference Synthesizer Block and whether the shielded jumper has failed or not between P9 and P21.

(b) 400 MHz ISO AMP
If the 400 MHz signal level of P21 is normal but if the signal level at pin 1 of C171 or pin 1 of C174 is −10 dBm or less, check the Q26, Q27, U61, and U62.

(c) MIX INPUT
If the output signal at pin 1 of C174 has the 400 MHz frequency and −10 dBm or higher level and if the signal level at pin 4 of MIX2 is −15 dBm or less, check the U59.

③ OFF IN check

(a) The OFF IF signal frequency can be determined by the following equation:
OFF IF frequency = (Frequency at pin 3 of MIX2) − (Frequency at pin 4 of MIX2)
If the signal having the OFF IF frequency with 0 dBm or higher level is not entered in pin 15 of U48, check the MIX2, LPF, U46, and U47.

④ Divider check in loop

(a) Data setup procedure
Check the offset signal division rate (=N) in the Maintenance mode, and determine the set value at addresses 440200 and 440210. For details, see the Maintenance mode section and each PLL control section of the synthesizer block.
Make sure that the U49 to U51 have been set to the set values correctly.

(b) Divider
If the correct data has been set for the divider but the TTL-level signals having the frequency (equal to the OFF IF frequency divided by N) are not entered in pin 13 of U40, check the divider.

⑤ Reference check

(a) 1/40 divider
If the 400 MHz frequency signal at −2 dBm or higher level is not entered in pin 2 of U43, check the U42. If the correct signal is entered in pin 2 of U43 but if the TTL-level 10 MHz signal is not entered in pin 4 of U45 although the signals are both high at pins 6 and 7 of U43, check the U43 and U44.

(b) 1/25 divider
If the TTL-level 400 kHz signal is not output at pin 6 of U41 although the correct signal is entered in pin 4 of U45, check the U45, U169, and U41.
Also, make sure that the signal has been set to low at pin 4 of U169 and that the signal has been set to high at pin 13 of U169.

⑥ Phase Detector check

Check the set frequency of Offset VCO in the Maintenance mode. Then, remove the R172 locating close to pin 4 of OFF VCO from the board, and connect the signal generator to the PAD connected to pin 2 of C136.
Set the signal generator as follows:

CW ..... Set frequency of Offset VCO
LEVEL 0dBm

Make sure that the TTL-level 400 kHz signals are entered in pins 1 and 13 of U40.
Monitor the signal at pin 5 of OFF VCO on the DVM and adjust the signal generator to have the value defined on Table 6-56.

Table 6-56 Voltage at Pin 5 of OFF VCO

SG Frequency Setup	Voltage at Pin 5 of OFF VCO
OFF VCO set freq. +100kHz	Approx. −12V
OFF VCO set freq. −100kHz	Approx. +12V

If the voltage at pin 5 of OFF VCO matches the one defined on Table 6-56, the Phase Detector operates normally.

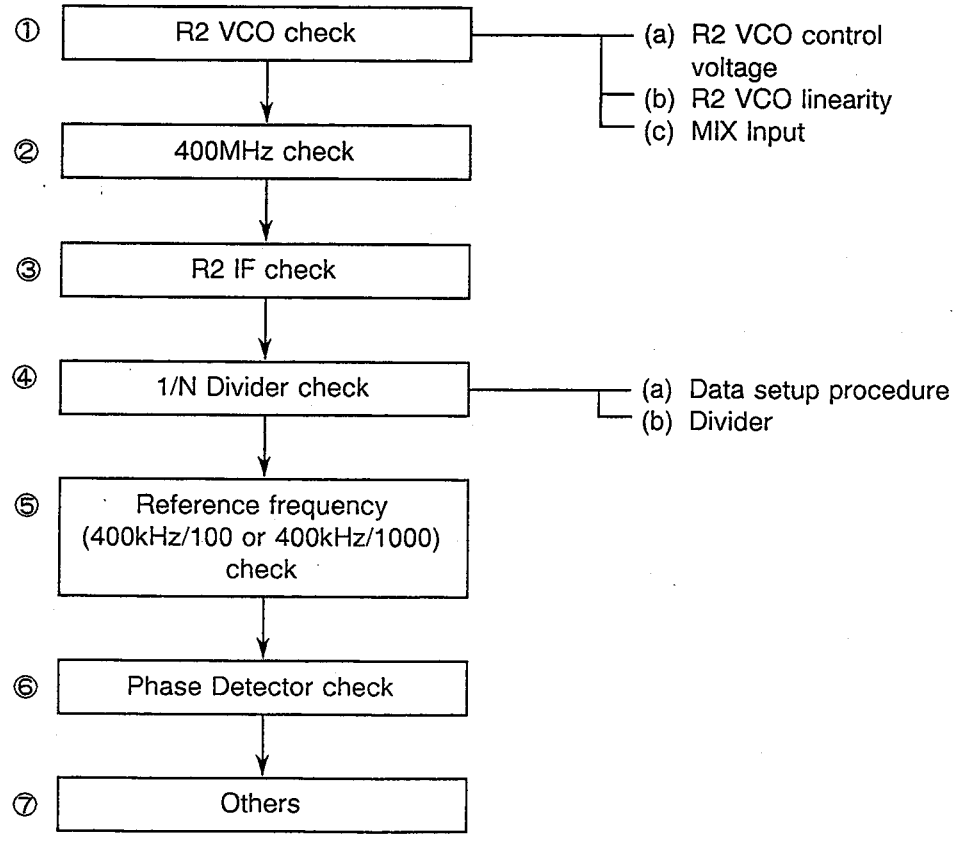
(6) Unlocked R2 PLL

If the measured oscillation frequency of the Reference PLL is the same as its set value but if the measured oscillation frequency of R2 PLL differs from its set value, use the following troubleshooting procedure.

The R2 PLL mixes the 400 MHz signal from the Reference PLL and the R2 VCO signal to generate an R2 IF signal. This signal is divided by "N", and this resulting signal and the 400 kHz signal sent from the Offset PLL, that is divided by 100 or 1000, are used for PLL lock. The R2 PLL has the Sample and Hold IC and uses the pretune voltage for signal sweep if 50 kHz ≧ SPAN > 200 Hz.

To check the unlocked PLL, select the SINGLE SWEEP mode. See the R2 block diagram of Figure 6-22.

The explanation is based on the following control flow:



① R2 VCO check

(a) R2 VCO control voltage

Set the R3265/3271 as follows:

CF 0Hz
SPAN 2MHz
SWEEP MODE ..... SINGLE

Make sure that approx. +7V appear at pins 6 and 7 of U151. At this time, the signal must be low at pin 8 of U151. If not, check the U151 and Q95.

(b) R2 VCO linearity

Remove the R65 (locating close to pin 1 of R2 VCO) from the board. Then, set the R3265/3271 as follows:

CF 0Hz
SPAN 2MHz
SWEEP MODE ..... SINGLE

Monitor the signal voltage at pin 4 of R2 VCO on the spectrum analyzer and monitor the signal at pin 2 on the DVM.
Select the Debug mode and enter data "0000" to "00ff" in address 440320 using the encoder. For details, see substep (b) of Step ① of "Unlocked R1 PLL" section.
Make sure that the signal voltage and frequency being monitored match the ones defined on Table 6-57.

Table 6-57 R2 VCO Linearity Check

Data	Voltage	Frequency
0000 to 00ff	+4.5V to −5.5V	345MHz to 420MHz

Also, make sure that the signal frequency changes according to the encoder value.
If the voltage is incorrect, see the "Pretune Linealizer" section. If the signal frequency is incorrect, the VCO may have failed.

(c) MIX Input

In the same status of substep (b) above, adjust the encoder to have the 370 MHz output signal frequency at pin 4 of R2 VCO. At this time, make sure that the output signal level is approx. +1 dBm at pin 4 of R2 VCO.
Make sure that the signal having the 370 MHz frequency with −10 dBm ±4 dBm appears at pin 4 of MIX1. If not, check the Q10, U34, and U35.

② 400 MHz check

Make sure that the signal having the 400 MHz frequency with +3 dBm or higher level is entered in pin 3 of MIX1. If not, check the Q11 and U37.

③ R2 IF check

Set the system in the same status as used in substep (b) of ①, and adjust the encoder to have the 370 MHz oscillation frequency of R2 VCO. Also, make sure that the signal having approx. 30 MHz frequency with +5 dBm or higher level is entered in pin 15 of U27. If not, check the MIX1, LPF, U25, and U26.

④ 1/N Divider check

(a) Data setup procedure
Check the set values in the Maintenance mode, and make sure that the correct set values have been set for U29 and U30. For details, see Item ⑦ of the table of "Maintenance mode" section. If the set value is incorrect, check the data line from U5 and U7 to the divider.

(b) Divider
If the correct data has been set for the divider but if the TTL-level signal (having the R2 IF frequency divided by N) is not entered in pin 13 of U21, check the divider.

⑤ Reference frequency (400 kHz/100 or 400 kHz/1000) check

Make sure that the 400 kHz, TTL-level signal is entered in pin 4 of U152. Also, check the following points.

Table 6-58 Reference Check

SPAN of R3265/3271	Voltage at Pin 2 of U153	Frequency at Pin 1 of U21
SPAN > 2 kHz	+5V	4kHz
SPAN ≦ 2 kHz	0V	400Hz

If the voltage at pin 2 of U153 does not match the one defined on Table 6-58, check the data line from U7 to U153.
If the signal frequency at pin 1 of U21 does not match the one defined on Table 6-58, check the U152, U153 and U31.

⑥ Phase Detector check

Display the CAL Menu on the R3265/3271 (by pressing the [SHIFT] and [CAL 7] keys simultaneously), and press the [CAL CORR ON/OFF] key to turn it off.
In the same status as substep (b) of ① above, adjust the encoder to have the 353.3 MHz oscillation frequency of R2 VCO. At this time, make sure that the 4 kHz signal is entered in pin 1 of U21 and that the roughly 4 kHz signal is entered in pin 13 of U21.
Monitor the signal at pin 3 of U24 on the DVM, and change the oscillation frequency of R2 VCO to the frequency given on Table 6-59 using the encoder.

Table 6-59 Voltage at Pin 3 of U24

Osc. Freq. of R2 VCO	Voltage at Pin 3 of U24
355MHz	Approx. −12V
350MHz	Approx. +12V

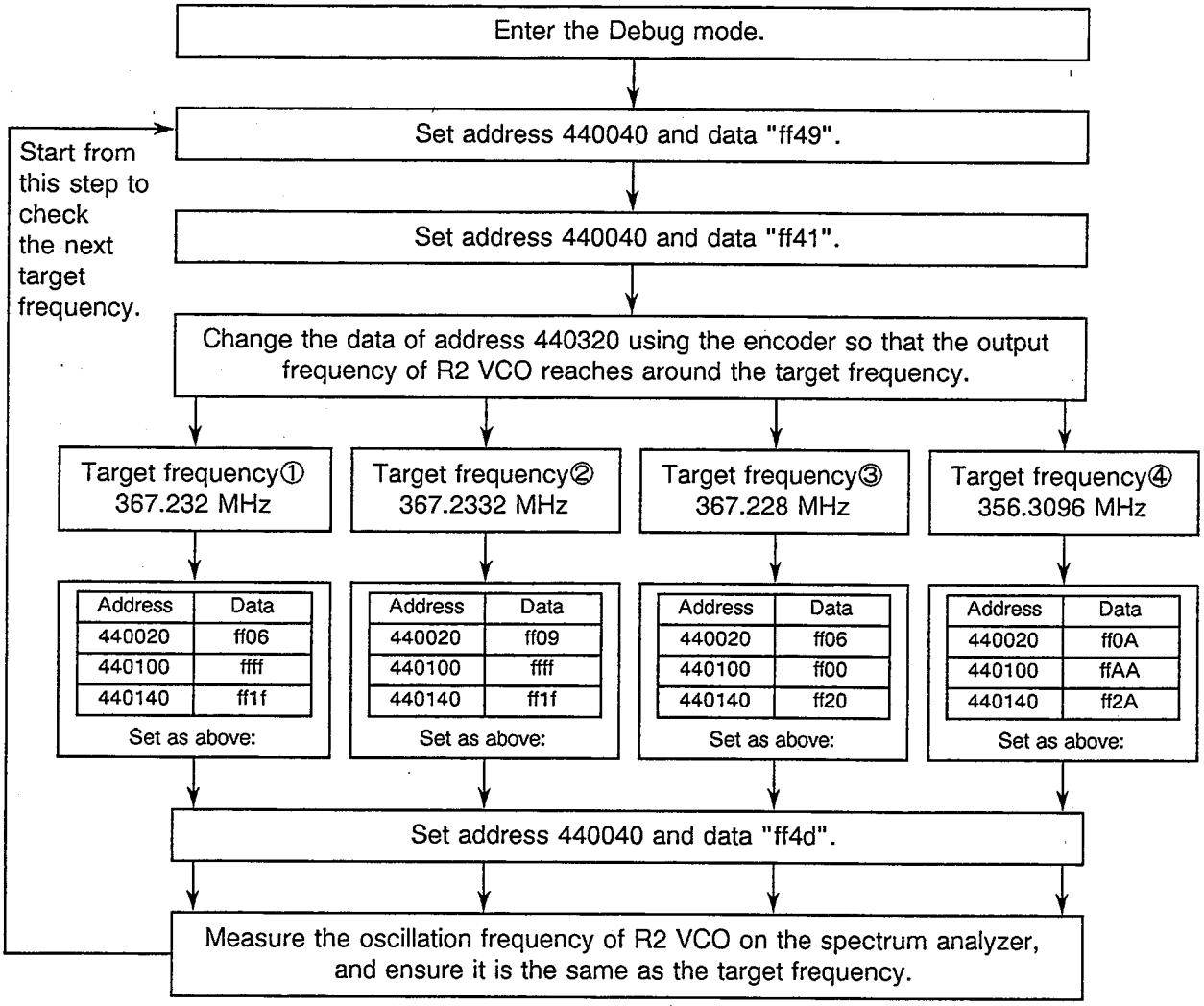
If the oscillation signal frequency can be changed to the one given on Table 6-59, the Phase Detector operates normally.

⑦ Digital IF mode

(a) If waveforms are deformed into step or concave format in the digital IF mode, the R2 PLL may have failed. The following explains how to isolate the cause of R2 PLL error.
First, set the R3265/3271 as follows:

CF 0Hz
SPAN ..... 2kHz (with Digital IF mode OFF)
SWEEP MODE ..... SINGLE

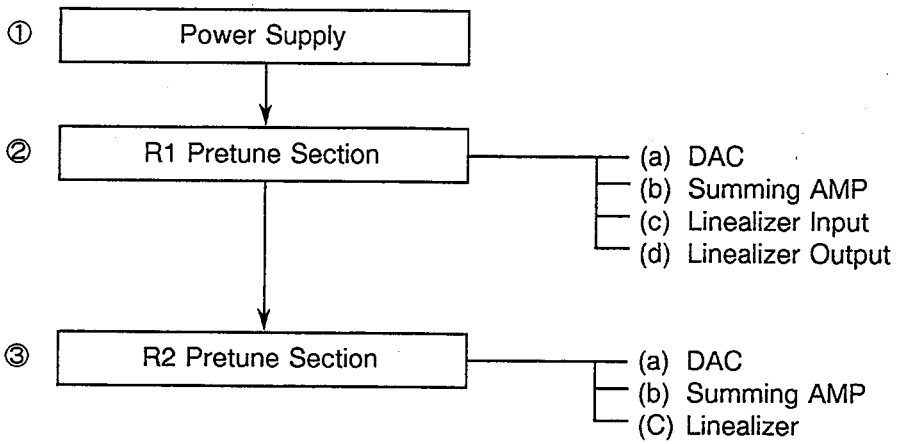
After a single sweep has completed, enter the Debug mode and perform the following procedure. During this time, monitor the output signal frequency at pin 4 of R2 VCO by using a spectrum analyzer synchronized with the R3265/3271.



Repeat the above procedure for all of four-type target frequencies. If the frequencies are the same, the R2 PLL operates normally.
If any of them fails, check the divider (U29, U28, U29, and U30), data latch (U5 and U7), and data line between the divider and data latch.

(7) Pretune, Linealizer, and Power Supply

The following explains the R1 and R2 pretune voltages or Linealizer. See the Linealizer and Pretune section of Figure 6-22. They are explained in the following sequence.



Set the R3265/3271 as follows and start troubleshooting.

CF 0MHz
SPAN 2MHz
SWEEP MODE ..... SINGLE

① Power Supply

The Synthesizer block primarily uses 3 types of signal voltages sent from the I/O block and generates 7 types of voltages. If one of these voltages has failed, the R1 or R2 PLL is unlocked. Table 6-60 summarizes the signal names on the circuit diagram, voltage measuring points, set voltages, and the troubleshooting points.

Table 6-60 Power Supply Check

Signal Name on Circuit Diagram	Voltage Measuring Point	Set Voltage	Troubleshooting Points
+4.6 V	Pin 2 of Q56	+4.6 V ± 0.2 V	Q56, U102
+5 DA	Pin 1 of Q100	+5 V ± 0.05 V	Q100, U156
+5 DB	Pin 7 of U101	+6.15 V ± 0.2 V	Q102, U101
+10 DA	Pin 1 of Q101	+10 V ± 0.05 V	Q101, U100
+14.5 DA	Pin 1 of Q98	+14.25 V ± 0.1 V	Q98, U101
−13.3 DB	Pin 3 of Q55	−13.15 V ± 0.2 V	Q55, U100
−13.3 DA	Pin 7 of U156	−8.4 V ± 0.1 V	U156, Q99

The voltages listed on Table 6-60 can be obtained only when the correct voltage is supplied from the I/O board (BLL-017508X03) to terminal J3 of Synthesizer Block. If the voltage at J3 is abnormal, check the I/O board (BLL-017508X03).

② R1 Pretune Section

Table 6-62 lists the voltages that appear at each part of R1 Pretune Section when the DAC (=U9) is set. However, the voltages at pins 3 and 6 of U16 may differ from the table values because they have been adjusted according to the R1 VCO characteristics. Set the DAC in the Debug mode as defined on Table 6-61.

Table 6-61 DAC Setup (at R1 Pretune Section)

DAC	Address	Data
DAC Ⓐ (=U9)	440330	ff0A to ffff
DAC Ⓑ (=U10)	4400A0	Fixed to ff00
DAC Ⓒ (=U10)	440080	Fixed to ff00

Note: Select the SINGLE SWEEP mode.

Set the fixed "ff00" data for DAC Ⓑ and DAC Ⓒ because they may affect very few on the pretune voltage.

Table 6-62 Voltages at Each Part of R1 Pretune Section

Data (HEX) of DAC Ⓐ	Output Voltage (Pin 7 of U13) of DAC Ⓐ	Output Voltage (Pin 6 of U15) of Summing AMP	Input Voltage (Pin 3 of U16) of Linealizer	Output Voltage (Pin 6 of U16) of Linealizer
ff0A	0.43 V	4.8 V	4.8 V	7 V
ff64	4.3 V	2.6 V	2.8 V	0.45 V
ffC8	8.6 V	0.15 V	0.9 V	−6.2 V
ffff	11 V	−1.2 V	−0.1 V	−10.2 V

(a) If the output voltage of DAC Ⓐ is incorrect:

- Make sure that approx. −11V are applied to pin 18 of U9.
- If OK, check the U9, U13, and data line.
  However, if the data line has failed, the output voltage of R2 Pretune DAC Ⓐ is also abnormal.

(b) If the output voltage of Summing AMP is incorrect:

- Make sure that the output voltage of DAC Ⓐ is applied to pin 1 of R6.
- Make sure that −13.15 ±0.2V are applied to pin 1 of R724.
- Make sure that the voltage is approx. 0 V at pin 1 of R7, at pin 1 of R10, and at pin 1 of R666.
- If the fault still continues, the U15 or D63 may have failed.

(c) If the input voltage of the Linealizer is incorrect:

- The D61 may have failed.

(d) If the output voltage of the Linealizer is incorrect:

- Make sure that −8.4 ±0.1V are applied to pin 1 of R669 and that +6.15 ±0.2V are applied to pin 1 of R615.
- If the above voltages are correct but the output voltage of Linealizer is still incorrect, the U16 may have failed.

③ R2 Pretune Section

Table 6-64 lists the voltages that appear at each part of R2 Pretune Section when the DAC (=U9) is set. However, the voltage at pin 6 of U164 may differ from the table value because it has been adjusted according to the R2 VCO characteristics.
Set the DAC in the Debug mode as defined on Table 6-63.

Table 6-63 DAC Setup (at R2 Pretune Section)

DAC	Address	Data
DAC Ⓐ (=U9)	440320	ff0A to ffff
DAC Ⓑ (=U10)	4400E0	Fixed to ff00
DAC Ⓒ (=U10)	4400C0	Fixed to ff00

Set the fixed "ff00" data for DAC Ⓑ and DAC Ⓒ because they may affect very few on the pretune voltage.

Table 6-64 Voltages at Each Part of R2 Pretune Section

Data (HEX) of DAC Ⓐ	Output Voltage (Pin 1 of U13) of DAC Ⓐ	Output Voltage (Pin 6 of U163) of Summing AMP	Output Voltage (Pin 6 of U164) of Linealizer
ff0A	0.43 V	2.45 V	4.1 V
ff64	4.3 V	0.76 V	0.6 V
ffC8	8.6 V	−1.1 V	−3.4 V
ffff	11 V	−2.1 V	−5.6 V

(a) If the output voltage of DAC Ⓐ is incorrect:

- Make sure that approx. −11V are applied to pin 4 of U9.
- If OK, check the U9, U13, and data line.
  However, if the data line has failed, the output voltage of R1 Pretune DAC Ⓐ is also abnormal.

(b) If the output voltage of Summing AMP is incorrect:

- Make sure that the output voltage of DAC Ⓐ is applied to pin 1 of R24.
- Make sure that −13.15 ±0.2V are applied to pin 1 of R668.
- Make sure that the voltage is approx. 0 V at pin 1 of R25, at pin 1 of R28, and at pin 1 of R667.
- If the fault still continues, the U163 may have failed.

(c) If the output voltage of the Linealizer is incorrect:

- Make sure that −8.4 ±0.1V are applied to pin 1 of R674 and that +6.15 ±0.2V are applied to pin 2 of R37.
- If the above voltages are correct but the output voltage of Linealizer is still incorrect, the U164 may have failed.

6.8.4 25 MHz CAL OUT Section

The signal sent from the 200 MHz VCXO (U1) is synchronized in its phase with the 10 MHz internal reference source. This signal is divided by 8 and the 25 MHz CAL OUT signal is obtained. This signal is output through saturation of Differential AMP. The 12-bit D/A Converter (BLS-017044, U103) of the constant-current circuit controls the operating current of the Differential AMP, and the 25 MHz CAL OUT signal level can be changed between −10 dBm and −30 dBm at each 0.5 dB step highly accurately. Also, all components, except for D/A Converter (U103) and Buffer AMP (U104), are mounted on the BLC-017046.

① If the 25 MHz CAL OUT signal level is outside the range of −10 dBm ±0.3 dBm, adjust it by rotating the R151 variable resistor. If it has failed, check the following:

- Measure the CAL voltage (potential between P1 and P11) that is applied to Ope AMP U12 of the constant-current circuit on the DVM. If the CAL voltage is outside the range of 9.988 ±20 mV, D/A Converter U103 and Buffer Amp U104 may have failed on the BLS-017044 board. Otherwise, the coaxial cable from Buffer AMP U104 to Ope AMP U12 may be open.

② The 25 MHz CAL OUT signal can be changed between −10 dBm and −30 dBm at each 0.5 dB step highly accurately. Use a highly sensitive sensor (having the 20 dB PAD) to read the 25 MHz CAL OUT signal for each set value on the power meter (*). When the 25 MHz CAL OUT signal is changed for 10 dB within the range of −10 to −25 dBm, the specifications show that its variation (called "step accuracy") must be within 10 dB ±0.03 dB. If this step accuracy does not match the specifications, check the following two points:

- Measure the input signal level that is entered in the base of NPN transistor Q12 (appearing as part of Differential AMP) on the spectrum analyzer, and log it. Set the spectrum analyzer as follows:

  CENTER FREQ 25MHz
  FREQ SPAN 1MHz

  Then, measure the 25 MHz IF OUT signal (at P3 of the circuit diagram) in the similar way and log it. If the input signal level to Q12 is 0 dBm or less and if the 25 MHz IF OUT signal level is 0 dBm or more, the U11 (AMP) may have failed. If the 25 MHz IF OUT signal is 0 dBm or less, the U8 (Divider) or U9 (AMP) may have failed.

- Change the 25 MHz CAL OUT signal level and measure the CAL voltage (potential between P1 and P11) applied to the U12 Ope AMP (appearing as part of the constant-current circuit) on the DVM. Compare this voltage with the logical values defined on Table 6-65, and if they differ more than ±20 mV, the U103 (D/A Converter) or U104 (Buffer AMP) may have failed on the BLS-017044 board.

Table 6-65 CAL Voltages

CAL OUT Signal Level (dBm)	CAL Voltage (mV)		Error (mV) bet. Logical and Measured Values
	Logical Value	Measured Value	
−10.0	9.988		
−10.5	9.431		
−11.0	8.906		
−11.5	8.410		
−12.0	7.941		
−12.5	7.499		
−13.0	7.081		
−13.5	6.687		
−14.0	6.315		
−14.5	5.964		
−15.0	5.632		
−15.5	5.319		
−16.0	5.024		
−16.5	4.745		
−17.0	4.481		
−17.5	4.232		
−18.0	3.998		
−18.5	3.776		
−19.0	3.567		
−19.5	3.369		
−20.0	3.183		
−20.5	3.007		
−21.0	2.840		
−21.5	2.684		
−22.0	2.535		
−22.5	2.396		
−23.0	2.263		
−23.5	2.139		
−24.0	2.021		
−24.5	1.910		
−25.0	1.805		
−25.5	1.706		
−26.0	1.613		
−26.5	1.525		
−27.0	1.441		
−27.5	1.363		
−28.0	1.288		
−28.5	1.218		
−29.0	1.152		
−29.5	1.090		
−30.0	1.031		

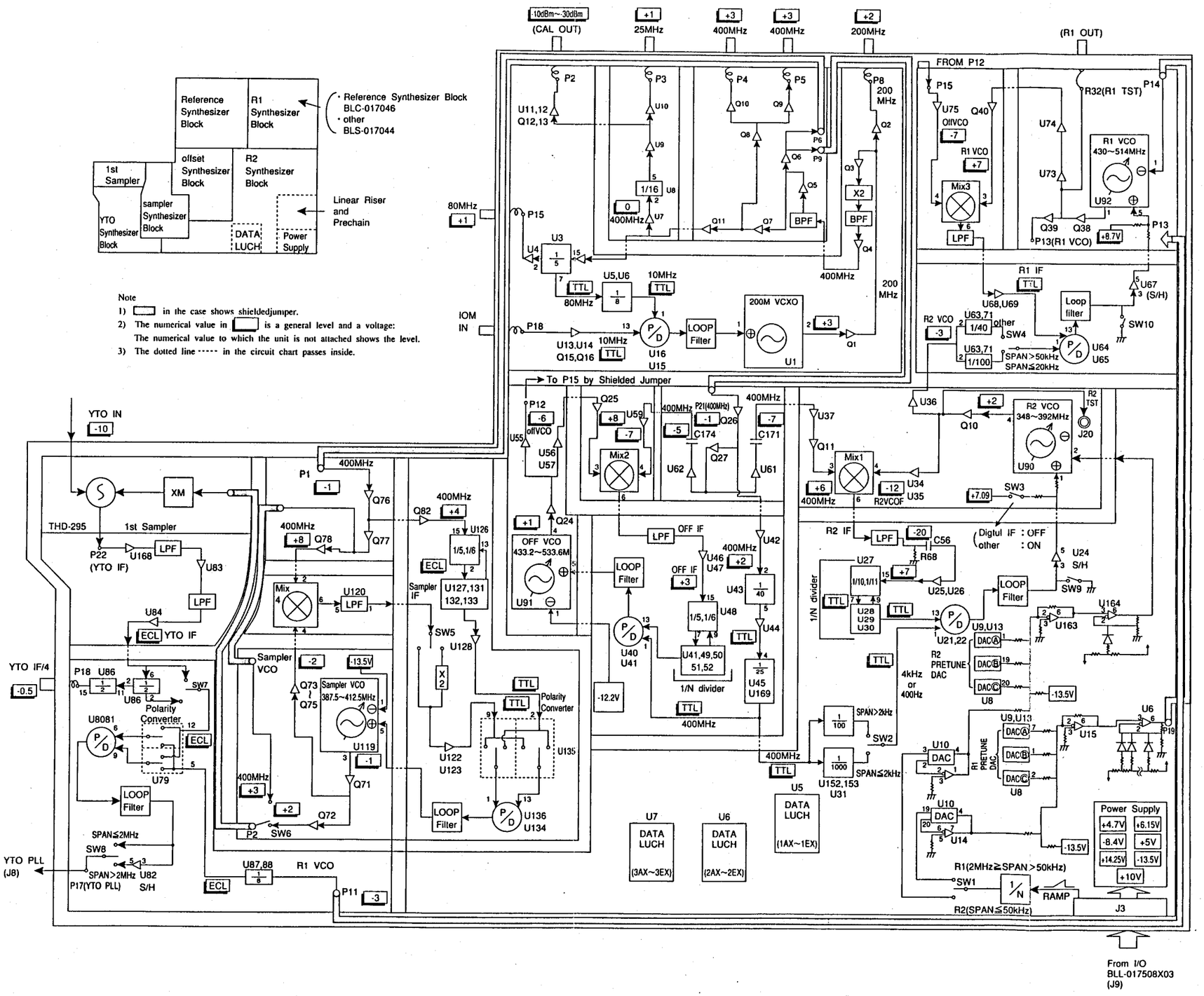


Figure 6-22 Synthesizer BLOCK DIAGRAM

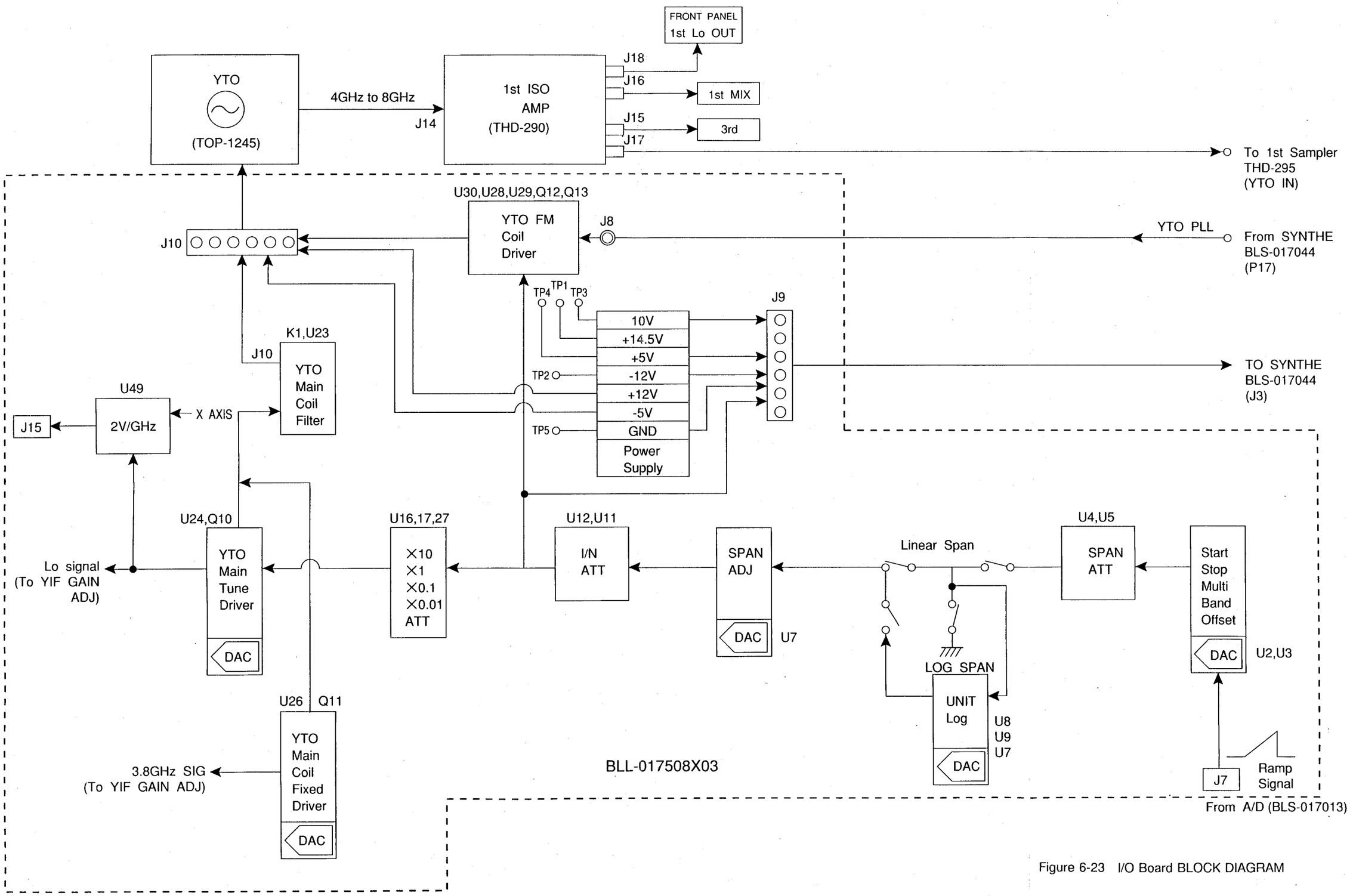


Figure 6-23 I/O Board BLOCK DIAGRAM

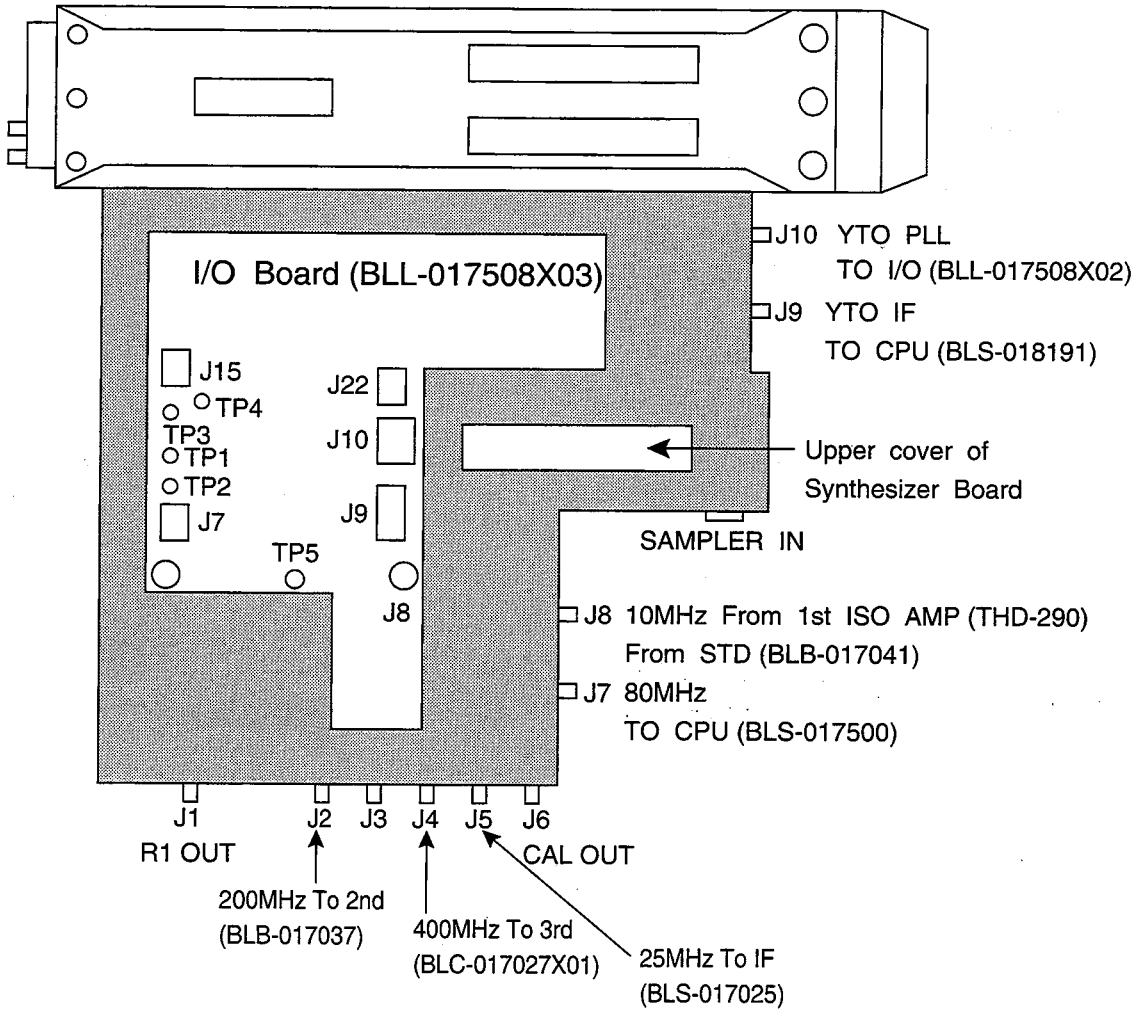
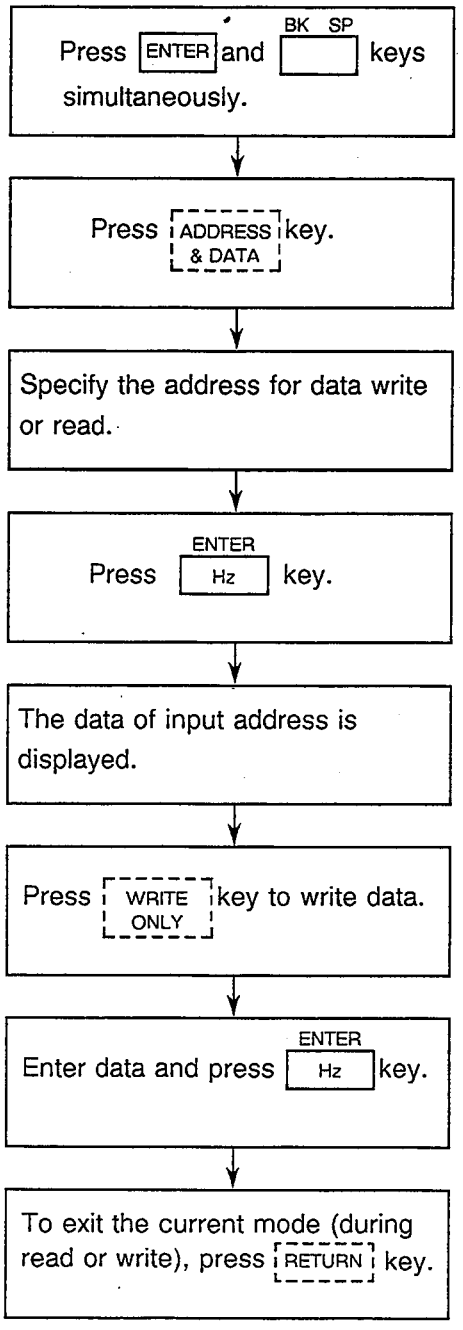


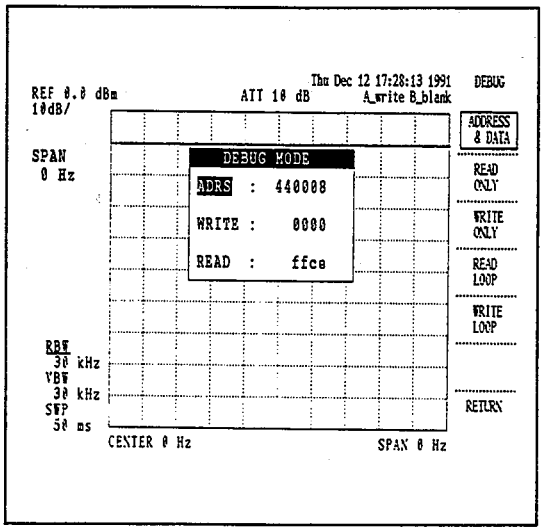
Figure 6-24 State to lay main body and to open Synthesizer Board

6.8.5 Appendix

(1) Each PLL control

Each PLL has various switches, and their switch (SW) setup and data change when the center frequency, span RBW and others are changed. This section explains the data of each synthesizer address.
First, specify the data to be read or written on the R3265/3271 screen (see the Debug mode section).





CAUTION

- If an incorrect data or address is entered, use the BK SP key to correct it.
- Because the data must be entered in the hexadecimal format during Debug mode, "A" to "F" need to be entered. The following lists the associated keys of the R3265/3271.

Table 6-66 Hexadecimal Data Key Assignment

Data (HEX)	R3265/3271 Keys
A	CENTER FREQ
B	FREQ SPAN
C	START
D	STOP
E	REF LEVEL
F	CPL

- When the data is read from the synthesizer, the data output by the latch (U5, U6, U7) of the synthesizer is read.
  Therefore, the set value of the CPU may not match the data read in the Debug mode. If it has occurred, check the data line.
- The data can be read from the synthesizer only when it is stored in the latch.
  The set data of Pretune DAC and Gain Correction DAC cannot be read.
- The data of 0 to 255 (decimal) can be entered in each synthesizer address.
  They are 0 to ff (hexadecimal). Therefore, the low-order 2 digits of (4-digit) data is effective in the Debug mode.
- If data is written in the synthesizer address, the set data of the CPU is written automatically between the time when the signal sweep of R3265/3271 ends and when the next sweep starts. To prevent automatic data writing from the CPU, select the SINGLE sweep mode (during lock after a single sweep) or select the MANUAL sweep mode.
- For the switch numbers (SW○) used in this section, see the diagram of Figure 6-22.

① YTO PLL

The following two addresses are used for YTO PLL:

440160 (440168 during data reading)

440110 (440118 during data reading)

- Address 440160

  The data is 8 bits long in hexadecimal notation.

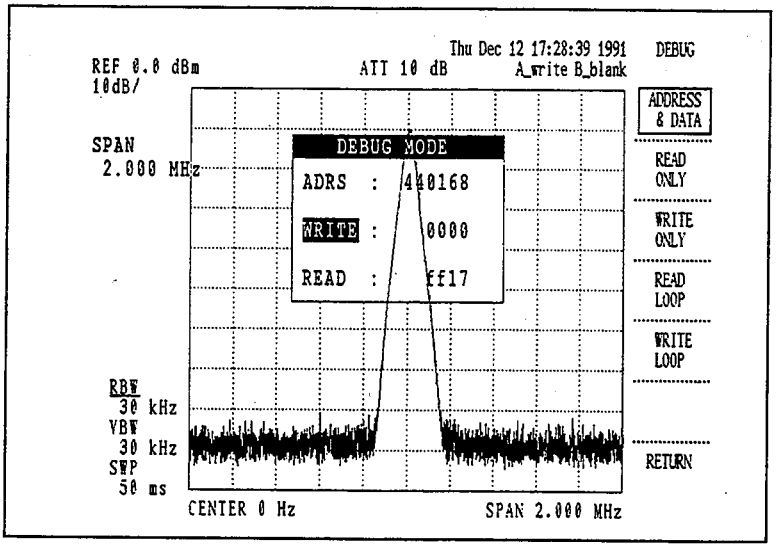
  Table 6-67 shows each bit setup.

Table 6-67 Each Bit Setup (at Address 440160)

Bit	Setup		
7	Divider switching in loop (SW7)	1:1/1 0:1/2	
6 5	Unused (normally 0)		
4	Loop filter	1: Narrow loop filter ON 0: Narrow loop filter OFF	If both bits 4 and 3 are 0's, the wide loop filter is used.
3	Loop filter	1: MID loop filter ON 0: MID loop filter OFF	
2	Polarity conversion (U79)	1: YTO IF = (Sampler PLL×M) −. YTO 0: YTO IF = YTO − (Sampler PLL×M)	
1	Sample and Hold	1: Sample (during YTO lock) 0: Hold (during YTO sweep)	
0	Use of R3265/3271 counter	1: Lack of YTO IF/4 output at P18 0: Output of YTO IF/4 output at P18	

Set the R3265/3271 as follows and read data from address 440160.

CF 0MHz
SPAN 2MHz
SWEEP MODE ..... CONT SWP



CAUTION

When reading data (for the synthesizer only), set the low-order 1 digit of address to "8".
Example: Address "440160" must be "440168".

The read data is "ff17" (HEX). If the low-order 2 digits of data is binary converted, they are 1 (H) = 0001 (B) and 7 (H) = 0111 (B). If they are assigned to the values of Table 6-67, the following can be obtained:

Table 6-68 Binary Data Conversion of 17 (HEX)

Bit	7	6	5	4	3	2	1	0
Hexadecimal	$1_{(H)}$				$7_{(H)}$			
Binary	0	0	0	1	0	1	1	1

It shows that the YTO loop is in the status as shown below.

Table 6-69 YTO Loop Status

Divide rate	1/2
Loop filter	Narrow
Polarity	YTO IF = (Sampler PLL × M) – YTO
S/H	Sample status
Counter	OFF

In the "Unlocked PLL" section, you are instructed to set bit 2 of Address 440xxx to 1. Set it as follows:

For example, to set bit 7 of Address 440160 high:

- Read data from Address 440160 (in the Debug mode).
- Convert the low-order 2 digits of this read data into binary format.
  If the read data is "ff17" (HEX), its binary data can be calculated from Table 6-68.

Bit	7	6	5	4	3	2	1	0
Binary	0	0	0	1	0	1	1	1

- If bit 7 is set to 1 and the data is converted into hexadecimal format:

Bit	7	6	5	4	3	2	1	0
Binary	1	0	0	1	0	1	1	1
Hexadecimal	9				7			

- Enter the data in the Debug mode as follows:

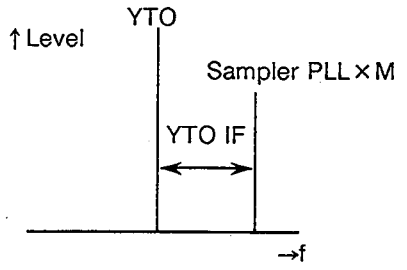
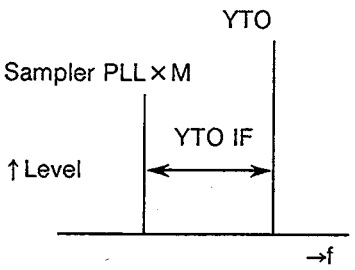
  Address 440160
  Data . . . . . ff97 (HEX)

Bit 7 of this data has been set to high.

The polarity conversion of bit 2 of Address 440160 means as follows:

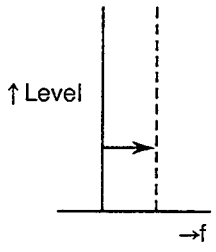
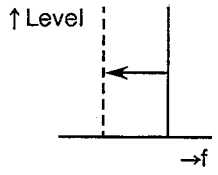
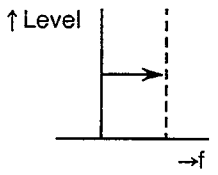
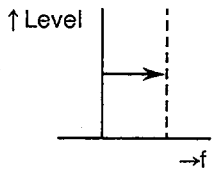
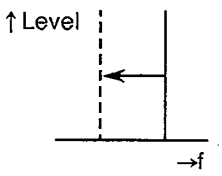
(a) Modification of YTO IF calculation
Table 6-70 provides the relationship between the YTO oscillation frequency when the PLL is locked, Sampler PLL multiplied by "M", and the YTO IF.

Table 6-70 YTO IF Calculation

Bit 2 of Address 440160	1	2
Frequency		
Calculation expression	YTO IF =(Sampler PLL×M)−YTO	YTO IF =YTO−(Sampler PLL×M)

(b) Signal sweep direction of R1 PLL and R2 PLL if the SPAN is 2 MHz or less
The signal sweep direction is changed for R1 PLL and R2 PLL according to the value of bit 2 of Address 440160 (see Table 6-71).

Table 6-71 Signal Sweep Direction for YTO R1 and R2

Bit 2 at 440160	YTO Sweep Direction	R1 (2 MHz≧ SPAN>50 kHz)	R2 (50 kHz≧SPAN>200 Hz)
1			
0			

Data of bits 2 and 7 at Address 440160 vary according to the center frequency. Also, bits 3 and 4 vary according to the SPAN setup.
The loop filter of bits 3 and 4 are usually set as follows:

Table 6-72 Loop Filter Setup (YTO PLL)

Span	Bit 4	Bit 3	Loop Filter
SPAN > 2 MHz	0	1	MID
2 MHz ≧ SPAN > 200 kHz	1	0	NARROW
200 kHz ≧ SPAN	0	0	WIDE

Only the YTO PLL loop filter changes in its status at the boundary of 200 kHz span.

- Address 440110
  This address is 4 bits long. In the Debug mode, the low-order 1 digit is effective.
  Table 6-73 defines each bit setup.

Table 6-73 Each Bit Setup (at Address 440110)

Bit	Setup	
3	Switching of YTO PLL voltage (TO I/O) (SW8)	1: YTO PLL voltage OFF 0: YTO PLL voltage ON
2		1: PLL voltage passing through U82 is OFF. 0: PLL voltage passing through U82 is ON.
1	Unused	
0	Switching of R2 PLL reference frequency to 4 kHz or 400 Hz (SW2)	1: 4kHz 0: 400Hz

- Bits 3 and 2 are used to sent send the YTO PLL voltage to the I/O passing through the Sample and Hold IC or not. See the YTO Synthesizer block diagram of Figure 6-22.
  This switching is associated with the SPAN setup.

Table 6-74 YTO PLL Voltage Switching by SPAN Setup

SPAN	Bit 3	Bit 2
SPAN > 2 MHz	1	0
SPAN ≦ 2 MHz	0	1

If the Sampler PLL or VHF PLL has been locked and if the YTO is locked or unlocked at the boundary of SPAN = 2 MHz, the SW8 specifying these bits may have failed.

- Bit 0 is used to switch the Reference frequency of R2 PLL.
  The Synthesizer block of Figure 6-22 relates to SW2.
  Also, this bit relates to the SPAN setup as follows:

Table 6-75 Switching of Reference Frequency by Bit 0

SPAN	Bit 0	Reference Frequency
SPAN > 2 MHz	1	4kHz
SPAN ≦ 2 MHz	0	400Hz

② Sampler PLL

The Sampler PLL uses the following 3 addresses:
440120 (440128 during data reading)
440220 (440228 during data reading)
440260 (440268 during data reading)
The divider of Sampler PLL has been set at addresses 440220 and 440260.
See the Sampler Synthesizer block diagram of Figure 6-22.

- Address 440120
  The data is 8 bits long in hexadecimal notation.
  Table 6-76 shows each bit setup.

Table 6-76 Each Bit Setup (at Address 440120)

Bit	Setup		
7 6	Unused		
5	Loop filter	1: MID loop filter ON 0: MID loop filter OFF	If both bits 5 and 4 are 0's, the wide loop filter is used.
4	Loop filter	1: Narrow loop filter ON 0: Narrow loop filter OFF	
3	Unused		
2	Doubler ON/OFF switching in loop (SW5)	1: ×1 0: ×2	
1	Switching of Sampler PLL OUT to 400 MHz or Sampler VCO (SW6)	1: PLL OUT = 400 MHz 0: PLL OUT = Sampler VCO	
0	Switching of Sampler VCO to above or below 400 MHz (U135)	1: 400 MHz or more 0: Below 400 MHz	

To check the logical set bit of data in Debug mode, refer to Address 440160 of the YTO PLL. Bits 0, 1 and 2 relate to the center frequency.
Bits 5 and 4 relate to the SPAN setup. The normal setup is defined on Table 6-77.

Table 6-77 Loop Filter Setup (Sampler PLL)

Span	Bit 5	Bit 4	Loop Filter
SPAN > 2 MHz	0	0	WIDE
160 kHz < SPAN ≦ 2 MHz	1	0	MID
SPAN ≦ 160 kHz	0	0	WIDE

Only the Sampler PLL loop filter is switched at the boundary of 160 kHz span.

- Addresses 440220 and 440260
  The divider set values are stored in these addresses.
  Check the accurate set values in the Maintenance mode.
  The details are explained in Item ④ of the table of "Maintenance Mode" section.

③ R1 PLL

The R1 PLL uses the following address:
Address 440000 (440008 during data reading in Debug mode)

- Address 440000
  Each bit setup is shown on Table 6-78. .

Table 6-78 Each Bit Setup (at Address 440000)

Bit	Setup		
7	Lamp signal polarity	1: Lamp voltage at pin 7 of U104:  0: Lamp voltage at pin 7 of U104: 	
6	Pretune filter	1: Narrow pretune filter ON 0: Narrow pretune filter OFF	
5	Switching of reference frequency (R2 PLL/40 or 100) (SW4)	1: R2 PLL/40 0: R2 PLL/100	
4	Pretune filter	1: MID pretune filter ON 0: MID pretune filter OFF	
3	Sample and Hold	1: Sample 0: Hold	
2	PLL ON/OFF (SW10)	1: PLL voltage = PLL voltage 0: PLL voltage = 0 V	
1	Loop filter	1: MID loop filter ON 0: MID loop filter OFF	If bits 1 and 0 are both 0's, the wide loop filter is used.
0	Loop filter	1: Narrow loop filter ON 0: Narrow loop filter OFF	

The lamp voltage polarity of bit 7 is switched according to bit 2 of YTO address 440160 and the SPAN setup as defined on Table 6-79

Table 6-79 Lamp Voltage Polarity of Bit 7

Bit 2 of 440160	SPAN	Bit 7 of 440000
1	2 MHz≧SPAN > 50 kHz	0
	50 kHz≧SPAN	1
0	2 MHz≧SPAN > 50 kHz	1
	50 kHz≧SPAN	0

For the sweep direction and others of R1 VCO and R2 VCO, see the explanation of bit 2 of Address 440160.

Bits 6 and 4 are pretune filter data and it relates to the RBW.

Table 6-80 Bits 6 and 4 Relating to RBW

RBW	Bit 6	Bit 4
RBW≧10 kHz	0	0
10 kHz>RBW≧1 kHz	0	1
RBW<1 kHz	1	0

If the MANUAL sweep mode has been selected, bit 6 is 1 and bit 4 is 0.

Bit 5 relates to the span as defined on Table 6-81.

Table 6-81 Switching of Reference Frequency of Bit 5

SPAN	Bit 5	Reference Frequency
SPAN>50 kHz	0	R2 PLL/100
20 kHz<SPAN≦50 kHz	1	R2 PLL/40
SPAN≦20 kHz	0	R2 PLL/40

Bit 3 specifies the Hold status during signal sweep if 2 MHz≧SPAN>50 kHz and during MANUAL sweep mode.
Otherwise, bit 3 specifies the Sample status.
Bits 1 and 0 specifies the loop filter as follows for all spans:
If bit 1 is 1 and bit 0 is 0, the MID loop filter is inserted.

④ OFFSET PLL

The Offset PLL uses the following 3 addresses:

440240 (440248 during data reading in Debug mode)
440200 (440208 during data reading in Debug mode)
440210 (440218 during data reading in Debug mode)

- Address 440240

  If data is indicated in the binary format, it is 8 bits long.
  Each bit setup is shown on Table 6-82.

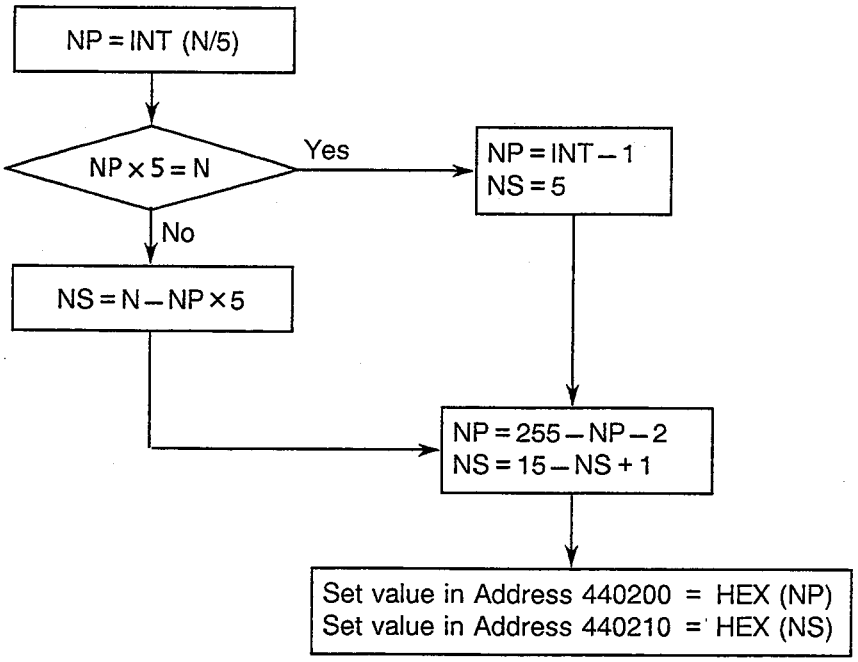
Table 6-82 Each Bit Setup (at Address 440240)

Bit	Setup	
7 6	Switching of Offset PLL reference frequency	Fixed to 0 Fixed to 1
5	Unused	
4 3 2 1 0	Loop filter NARROW ↓ WIDE Loop filter is ON if bit is 1.	All 0's specifies the most wide filter.

The fixed value must always be set for bits 7 and 6.
Bits 0 to 4 relate to the signal span and frequency.

- Addresses 440200 and 440210
  The divider set values are set in these addresses.
  Check the accurate set values in the Maintenance mode.
  The details are explained in Item ⑥ of the table of "Maintenance Mode" section.

  If N = Offset PLL division rate, the set value can be determined in the following flow chart.



⑤ R2 PLL

The R2 PLL uses the following addresses:

440040 (440048 during data reading in Debug mode)
440020 (440028 during data reading in Debug mode)
440100 (440108 during data reading in Debug mode)
440140 (440148 during data reading in Debug mode)
440110 (440118 during data reading in Debug mode)

- Address 440040

  Each bit setup is shown on Table 6-83.

Table 6-83 Each Bit Setup (at Address 440040)

Bit	Setup	
7	Switching of PLL voltage ratio to VCO to 1/1 or 10/1 (SW3)	1: 1/1 (during Digital IF) 0: 10/1 (during Normal Span)
6	Pretune filter	1: ON (RBW≦100 Hz or MANUAL Sweep) 0: OFF (RBW > 100 Hz)
5	Loop filter	1: ON (Digital IF or SPAN≦2 kHz) 0: OFF
4	Loop filter	1: ON (Digital IF) 0: OFF
3	Sample and Hold	1: Sample 0: Hold
2	PLL ON/OFF (SW9)	1: PLL voltage = PLL voltage 0: PLL voltage = 0 V
1	Loop filter	1: Narrow loop filter ON 0: Narrow loop filter OFF
0	Loop filter	1: MID loop filter ON 0: MID loop filter OFF

The loop filter specified by bits 5 and 6 is used in the special case.

An example of application in the Digital IF mode. Usually, the MID loop filter (bit 0 is 1) is used.

The Sample and Hold of bit 3 is set to the Hold status (bit 3 is 0) if 50 kHz≧SPAN>200 Hz (except for Digital IF mode) or in the Manual Sweep mode. Otherwise, it is set to the Sample status.

- Addresses 440020, 440100, and 440140
  The divider data has been set in these addresses.
  Check the accurate set values in the Maintenance mode.
  The details are explained in Item ⑦ of the "Maintenance Mode" section.

- Address 440110
  The reference frequency switching data of R2 PLL is stored in this address.
  For details, see the explanation of Address 440110 of the "YTO PLL" section.

(2) Lamp voltage 1/N attenuator

The 1/N attenuator uses the following addresses:
440010 (440018 during data reading in Debug mode)
440020 (440028 during data reading in Debug mode)

The low-order 4 bits of data is used to store the R2 PLL divide ratio in address 440020.

- Address 440010
  Each bit setup is shown on Table 6-84.
  Only the low-order 4 bits of this address are effective.

Table 6-84 Each Bit Setup (at Address 440010)

Bit	Setup	
3	Send of lamp voltage to R2 VCO	1: R2 VCO does not sweep. 0: R2 VCO does sweep.
2	Send of lamp voltage to R1 VCO	1: R1 VCO does not sweep. 0: R1 VCO does sweep.
1	1/10 ATT switching	1: 1/10 ATT is turned OFF. 0: 1/10 ATT is turned ON.
0	1/1 ATT switching	1: 1/1 ATT is turned OFF. 0: 1/1 ATT is turned ON.

Table 6-85 lists the set values of each span at Address 440010.

Table 6-85 Set Values of Each Span

SPAN	Hex Data at 440010
Digital IF if SPAN > 2 MHz	1 (H)
2 MHz ≧ SPAN > 400 kHz	A (H)
400 kHz ≧ SPAN > 50 kHz	9 (H)
50 kHz ≧ SPAN > 20 kHz	6 (H)
20 kHz ≧ SPAN > 2 kHz	6 (H)
2 kHz ≧ SPAN ≧ 200 Hz	5 (H)

- Address 44020
  If bit 6 of this address data is 0, the 1/5 ATT is inserted.
  At this time, the 1/1 ATT and 1/10 ATT must be ON at Address 440010.
  Also, the 1/5 ATT is inserted if bit 7 is 1 (the divider of YTO PLL has 1/1 ATT) at Address 440160 of YTO PLL and if 400 kHz ≧ SPAN > 50 kHz.

(3) Relationship between each address and latch
Table 6-86 provides the relationship between each address and latch.

Table 6-86 Relationship between Each Address and Latch

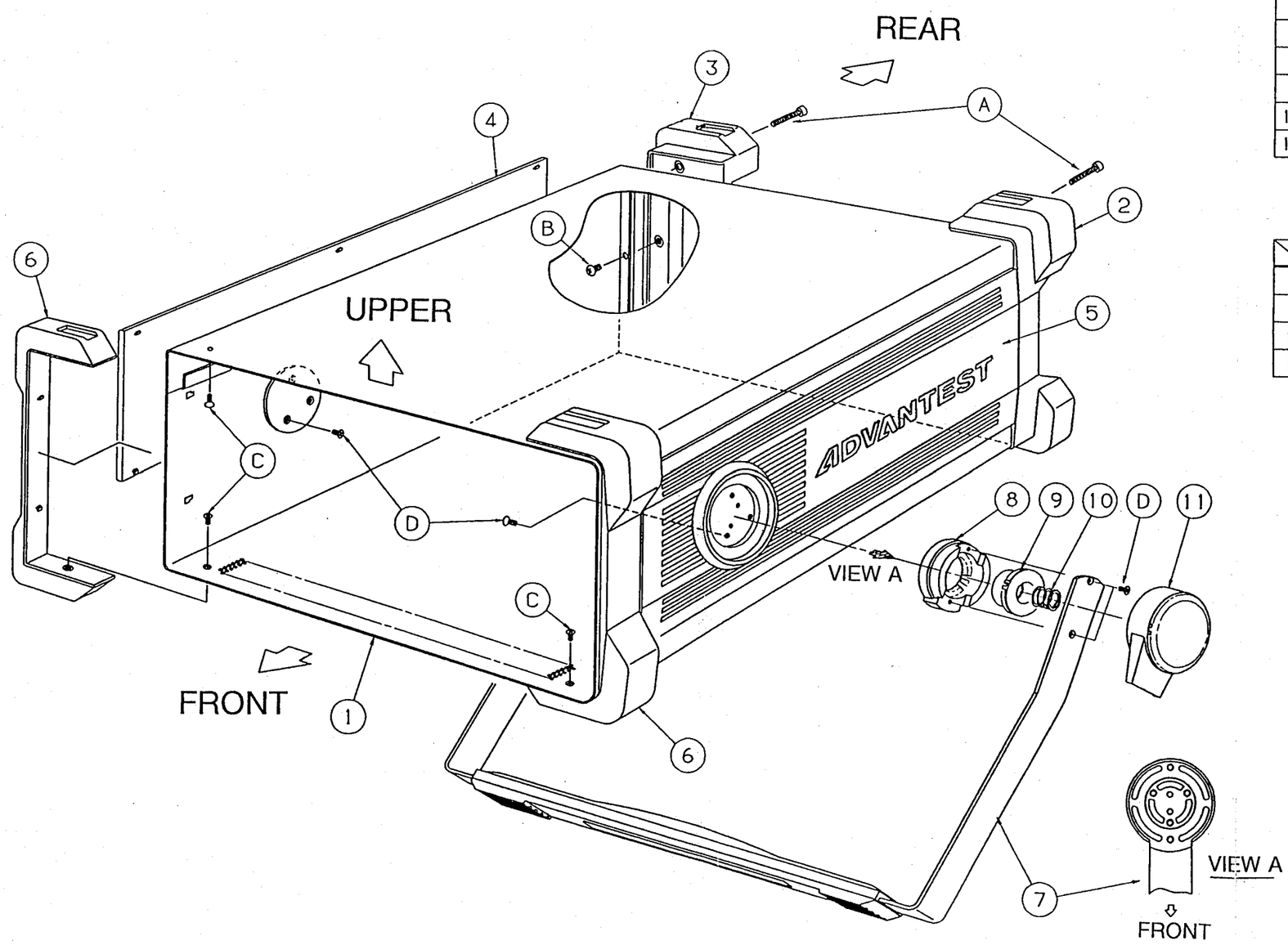
Address	Primary Function	Latch Part No.	Signal Name on Circuit Diagram
440000 440040 440020 440010	R1 PLL SW R2 PLL SW R2 PLL N Lamp signal switching	U5	1A0 to 1A7 1B0 to 1B7 1C0 to 1C7 1E0 to 1E3
440200 440240 440220 440260 440210	Offset PLL N Offset PLL SW Sampler PLL N Sampler PLL N Offset PLL N	U6	2A0 to 2A7 2B0 to 2B7 2C0 to 2C7 2D0 to 2D3 2E0 to 2E3
440100 440140 440120 440160 440110	R2 PLL N R2 PLL N Sampler PLL SW YTO PLL SW TYO PLL SW	U7	3A0 to 3A7 3B0 to 3B5 3C0 to 3C7 3D0 to 3D7 3E0 to 3E3

The low-order 1 bit of the signal name of the circuit diagram corresponds to each bit explained above.

MEMO

7. REPLACEABLE MECHANICAL PARTS

EXPLODED VIEW 1

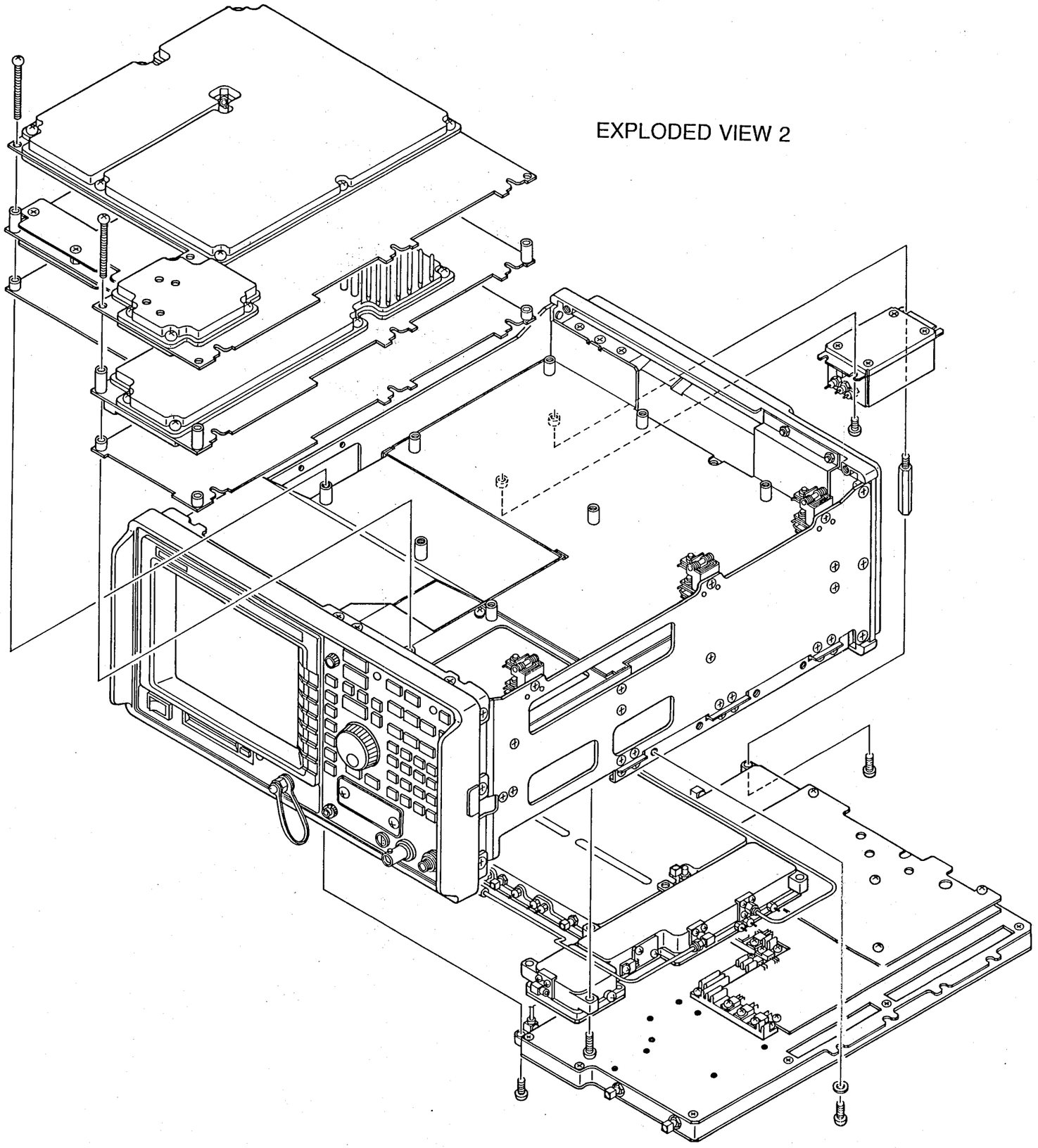


	Description	CODE	Q'ty
1	CABINET	MBX-69394	1
2	DUNPER, REAR L	MMX-69397	1
3	DUNPER, REAR R	MMX-69398	1
4	COVER, SIDE L	MMS-69377	1
5	COVER, SIDE R	MMS-69378	1
6	DUNPER, F	MMX-69395	2
7	HANDLE, A	MME-69393	1
8	HUB	MCE-90308	2
9	RING, HANDLE	MCE-83731	2
10	SPRING	MEX-95207	2
11	COVER, HANDLE	MMS-69380	2

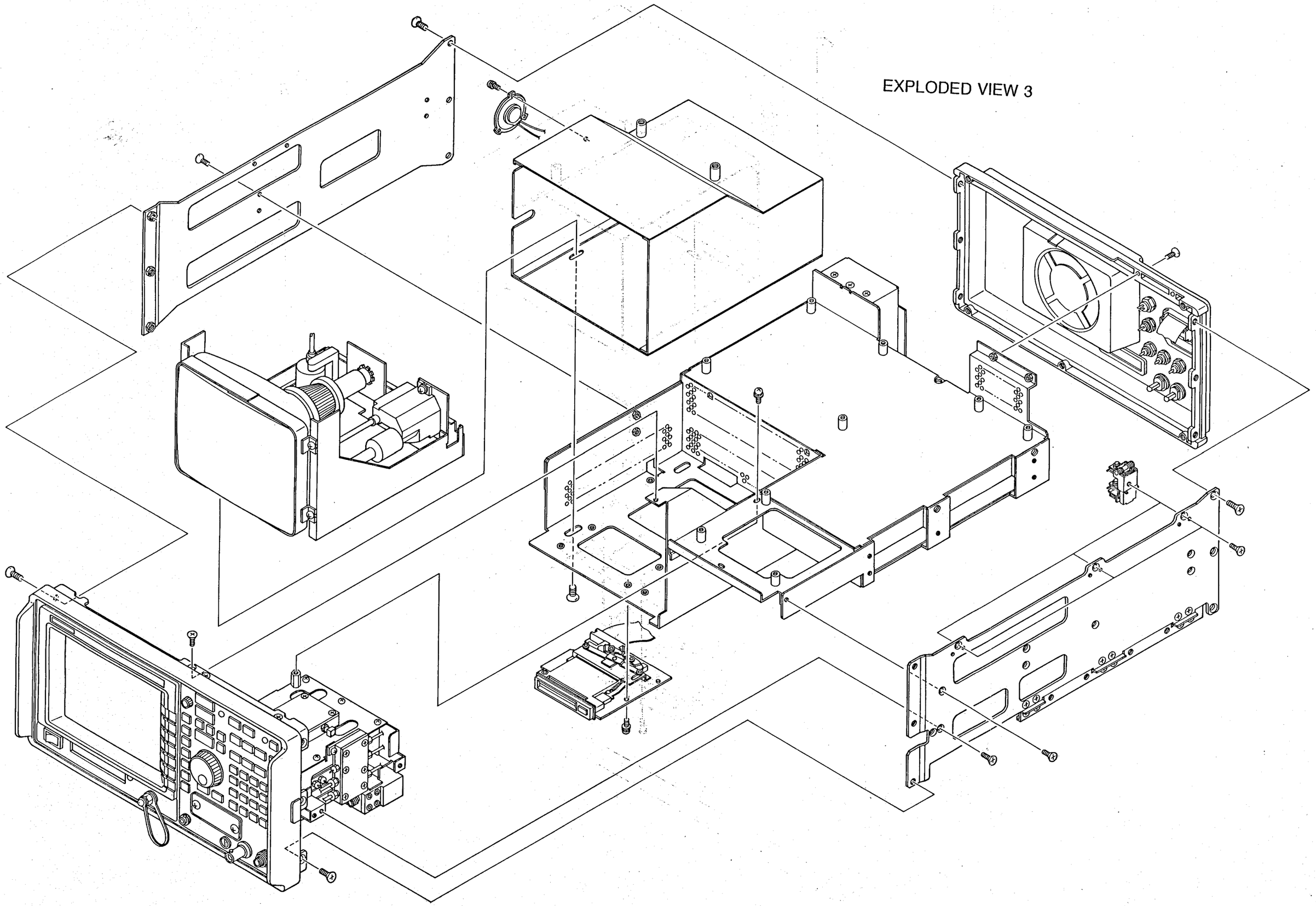
	Description	CODE	Q'ty
A	SCREW, HD4×30mm	YKG-H04894	4
B	SCREW, M4×8mm, RND	YKG-NB4X8	2
C	SCREW, M4×8mm, FLH	YKG-SB4X8	4
D	SCREW, M4×10mm, MECK	YKG-E001510	10

MODEL
R3265/71

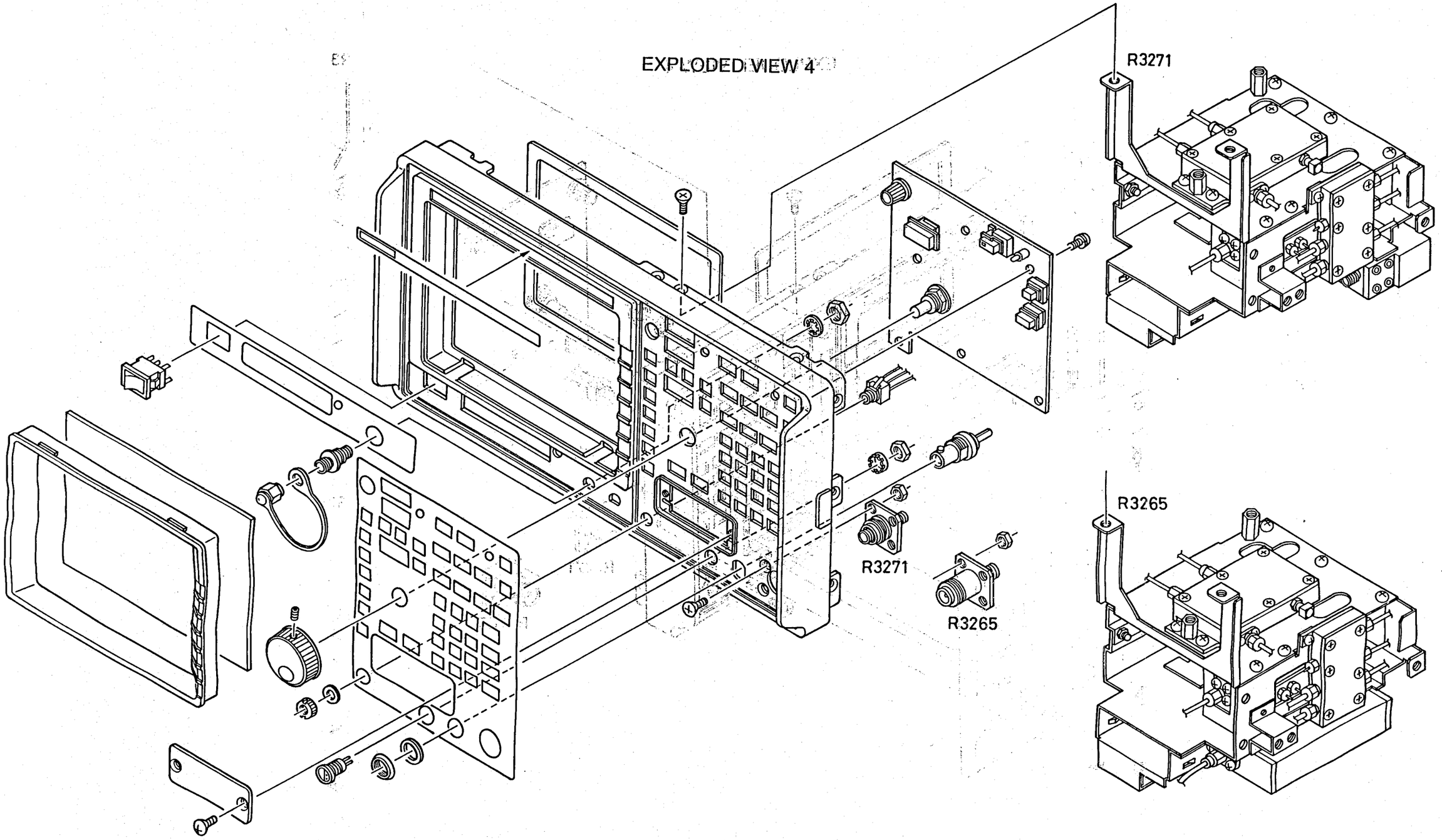
EXPLODED VIEW 2



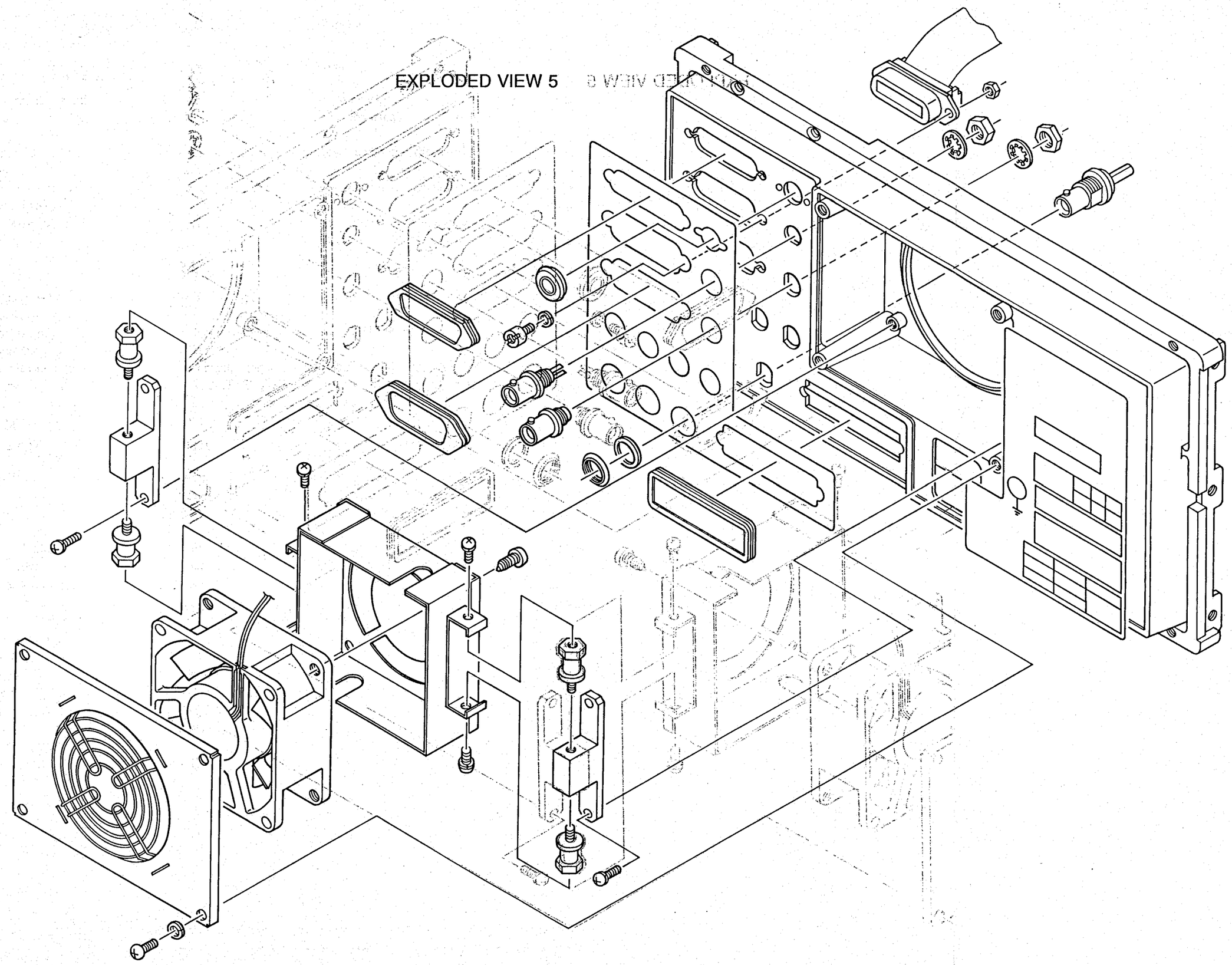
EXPLODED VIEW 3



EXPLODED VIEW 4



EXPLODED VIEW 5



WARRANTY

ADVANTEST product is warranted against defects in material and workmanship for a period of one year from the date of delivery to original buyer.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by buyer, unauthorized modification or misuse, accident or abnormal conditions of operations.

No other warranty is expressed or implied. ADVANTEST specifically disclaims the implied warranties of merchantability and fitness for a particular purpose.

ADVANTEST shall not be liable for any special incidental or consequential damages, whether in contract, tort or otherwise.

Any and all warranties are revoked if the product is removed from the country in which it was originally purchased.

SERVICE

During the warranty period, ADVANTEST will, at its option, either repair or replace products which prove to be defective.

When trouble occurs, buyer should contact his local supplier or ADVANTEST giving full details of the problem and the model name and serial number.

For the products returned to ADVANTEST for warranty service, buyer shall prepay shipping and transportation charges to ADVANTEST and ADVANTEST shall pay shipping and transportation charges to return the product to buyer. However, buyer shall pay all charges, duties, and taxes incurred in his country for products returned from ADVANTEST.

CLAIM FOR DAMAGE IN SHIPMENT TO ORIGINAL BUYER

The product should be thoroughly inspected immediately upon original delivery to buyer. All material in the container should be checked against the enclosed packing list or the instruction manual alternatively. ADVANTEST will not be responsible for shortage unless notified immediately.

If the product is damaged in any way, a claim should be filed by the buyer with carrier immediately. (To obtain a quotation to repair shipment damage, contact ADVANTEST or the local supplier.) Final claim and negotiations with the carrier must be completed by buyer.

SALES & SUPPORT OFFICES

Advantest(Singapore)Pte.Ltd.
438A Alexandra Road
#08-03/06 Alexandra Technopark Singapore 119967
Phone : 65-274-3100 Facsimile : 65-274-4055

ROHDE & SCHWARZ Engineering and Sales GmbH
Mühldorfstr. 15 (P.O.B. 80 1429, D-81614 Munichen)
D-81671 Munichen, Germany
Phone : 49-89-4129-13711 Facsimile : 49-89-4129-13723

TEKTRONIX INC.
P.O. Box 500, M/S 39-520, Beaverton, Oregon 97077-0001
or
Howard Vollum Industrial Park, M/S 58-743, Beaverton, OR, 97077, U.S.A.
Inside the U.S. 1-800-426-2200
Outside the U.S. 1-503-627-1933

—— Technology Support on the Leading Edge ——
ADVANTEST®
ADVANTEST CORPORATION
Shinjuku-NS Building, 4-1, Nishi-Shinjuku 2-chome, Shinjuku-ku, Tokyo 163-0880, Japan
Phone:+81-3-3342-7500 Facsimile:+81-3-5322-7270 Telex:232-4914 ADVAN J